CBCS SCHEME

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18MT35

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain with neat diagram and wave form biased positive clippers. **(06 Marks)**

b. Explain double ended shunt clippers with neat diagram and waveforms. **(06 Marks)**

c. Explain with neat diagram and frequency response, the working of RC coupled BJT amplifier. **(08 Marks)**

OR

2 a. Design a first order Butterworth high pass filter with cutoff frequency of 1KHz and pass band gain of 2. Plot the frequency response. Choose C =0.01μf. **(12 Marks)**

b. Explain with neat circuit diagram and waveform the working of wideband pass filter. **(08 Marks)**

Module-2

3 a. Design and explain the working of RC phase shift oscillator for f_0 = 200Hz. **(10 Marks)**

b. What is an oscillator? Mention the conditions required for sustained oscillation and also explain the working of Wein bridge oscillator. **(10 Marks)**

OR

4 a. What is comparator? With a neat diagram and waveform explain zero crossing detector. **(10 Marks)**

b. Explain the working of inverting comparator as Schmitt trigger with necessary waveforms. **(10 Marks)**

Module-3

5 a. Explain with neat diagram and waveform, the working of monostable multivibrator and also derive the expression for pulse width. **(12 Marks)**

b. Explain any one application of Astable multivibrator. **(08 Marks)**

OR

6 a. Explain with neat diagram and waveform the working of Astable multivibrator, and also derive equation for total time and duty cycle. **(10 Marks)**

b. Design an Astable multivibrator using 555 timer to generate clock of 1KHz with 60% duty cycle. Modify the circuit designed to obtain a clock of 1KHz with 40% duty cycle. Choose C = 0.01μf. **(10 Marks)**

Module-4

7 a. Using K – Map solve.
i) $P = f(r, s, t, u) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$
ii) $G = f(a, b, c, d) = \pi(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$. **(06 Marks)**
b. Implement $f(A, B, C) = \Sigma m(1, 3, 5, 6)$ using 4 : 1 MUX. **(06 Marks)**
c. Explain with logic diagram and truth table the full adder circuit. Also implement full adder using two 4 : 1 MUX. **(08 Marks)**

OR

8 a. What is a decoder? With logic diagram and truth table explain 3 to 8 line decoder. **(08 Marks)**
b. Design BCD to decimal decoder circuit. **(08 Marks)**
c. Implement full adder circuit using decoder and two OR gates. **(04 Marks)**

Module-5

9 a. With a neat circuit, analyze the operation of clocked JK flipflop and also derive the characteristic equation from truth table. **(10 Marks)**
b. Design a BCD ripple counter with : i) state diagram ii) logic diagram iii) Timing diagram. **(10 Marks)**

OR

10 a. Explain 3–bit synchronous binary up-down counter. **(10 Marks)**
b. With a neat circuit, analyze the operation of clocked RS flip-flop and also derive the characteristics equation from truth table. **(10 Marks)**

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