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10EE752

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Programmable Logic Controller

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1 a. What is PLC? Explain internal architecture of PLC with a neat block diagram showing bus connection. Mention its advantages. **(14 Marks)**
   b. Explain with relevant figures the following terms, with respect to performance of sensors:
      (i) Non linearity error   (ii) Hysterisis error. **(06 Marks)**

2 a. What is ladder diagram? Explain the conventions to be followed while drawing the ladder diagram. **(08 Marks)**
   b. Explain the concept of Latch circuit with an example. **(04 Marks)**
   c. Discuss the location of stop and emergency stop switches in a safe system. **(08 Marks)**

3 a. Show the ladder diagram, instruction list program implementation of OR-gate, NOR-gate and NAND-gate. **(06 Marks)**
   b. Design a system in which a valve is to be operated to lift a load when a pump is running and either the lift switch or a switch indicating that the load has not already been lifted and is at the bottom of its lift channel is operated. Draw the ladder diagram and functional block diagram. **(08 Marks)**
   c. For the instructions shown, draw the equivalent ladder diagram.

	(i)			(ii)	LDI	X400
	LD	X400			ANI	X401
	OR	X402			ANI	X402
	AND	X401			ANI	X403
	OUT	M100			OUT	Y430
	LD	M100			END.	
	AND	X403				
	OUT	Y430				

(06 Marks)

4 a. Define sequential function chart (SFC) and explain its elements. **(06 Marks)**
   b. Explain the conditional and iteration statement with proper syntaxes. **(10 Marks)**
   c. Explain the jump within jump operations with the help of an example. **(04 Marks)**

PART – B

5 a. Explain one shot operaton with necessary ladder diagram. **(06 Marks)**
   b. Explain the concept of Battery-Backed relays in PLC operation. **(06 Marks)**
   c. With neat ladder diagram and instruction list, explain Master Control Relay. **(08 Marks)**

6 a. Explain the three different forms of timers with timing diagrams. **(06 Marks)**
   b. Construct the ladder diagram, for possible traffic light sequence implementation. Write the sequential function chart and explain for the same. **(08 Marks)**
   c. Develop the ladder diagram with two cascaded timers, each having a delay time of 10 sec and 50 sec respectively. Write the instructions for the same with timing diagram. **(06 Marks)**

7 a. Write a note on up-counter, down counter with necessary ladder diagram. (06 Marks)
   b. Explain the use of counter to extend the range of timer. (08 Marks)
   c. Explain drum sequences in PLC. (06 Marks)

8 a. With the ladder diagram and instruction list show implementation of 4 bit shift register. (10 Marks)
   b. Explain different methods by which the controller can react to an error signal. (10 Marks)

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