CBCS SCHEME

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18EE34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronics Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. **(10 Marks)**

b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero. **(10 Marks)**

OR

2 a. Derive the expression for stability factors S′ and S″ for fixed bias circuit. **(08 Marks)**

b. A voltage divider biased circuit has $R_1 = 39K\Omega$, $R_2 = 82K\Omega$, $R_C = 3.3K\Omega$, $R_E = 1K\Omega$ and $V_{CC} = 18V$. The silicon transistor used has $\beta = 120$. Find Q-point and stability factor. **(07 Marks)**

c. Explain the operation of transistor as switch with suitable circuit and necessary waveforms. **(05 Marks)**

Module-2

3 a. State and prove Millers theorem. **(06 Marks)**

b. Compare the characteristics of CB, CE and CC configurations. **(06 Marks)**

c. For the collector feedback configuration having $R_F = 180K\Omega$, $R_C = 2.7K\Omega$, $C_1 = 10\mu F$, $C_2 = 10\mu F$, $\beta = 200$, $r_0 = \infty\Omega$ and $V_{CC} = 9$volts. Determine the following parameters:
i) re ii) z_i iii) z_o iv) A_v **(08 Marks)**

OR

4 a. Derive suitable expression to explain the effect of cascading of amplifiers on lower and upper cut off frequencies. **(08 Marks)**

b. Derive equations for miller input capacitance and miller output capacitance. **(08 Marks)**

c. A transistor in CE mode has h-parameters $h_{ie} = 1.1K\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. **(04 Marks)**

Module-3

5 a. Derive expression for Zi and Ai for a Darlington Emitter follower circuit. **(10 Marks)**

b. Explain the need of a cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

c. Write a note on cascade amplifier. **(04 Marks)**

OR

6 a. List the general characteristics of negative feedback amplifier. **(04 Marks)**

b. A given amplifier arrangement has the following voltage gain $AV_1 = 10$, $AV_2 = 20$ and $AV_3 = 40$. Calculate the overall voltage gain and determine the total voltage gain in dBS. **(08 Marks)**

c. For the voltage series feedback amplifier. Derive an expression for output impedance (Resistance). **(08 Marks)**

Module-4

7 a. Show that maximum efficiency of class-B push pull amplifier (power amplifier) circuit is 78.54%. **(08 Marks)**

b. Explain the classification of power amplifier with a neat circuit diagram and waveforms. **(07 Marks)**

c. A class-B push pull amplifier operating with $V_{CC} = 25V$ provides a 22V peak signal to 8Ω load. Calculate the circuit efficiency and power dissipated per transistor. **(05 Marks)**

OR

8 a. Draw the circuit of wein bridge oscillator and explain its operation. **(10 Marks)**

b. With a neat circuit diagram and waveform, explain the working principal of crystal oscillator operating in series resonant mode. A crystal has the following parameters L = 0.334H, C = 0.065pF and R = 5.5KΩ. Calculate its resonant frequency. **(10 Marks)**

Module-5

9 a. With the help of neat diagram, explain the working and characteristics of N-channel JFET. **(10 Marks)**

b. For a self bias JFET circuit, $V_{DD} = +12V$, $R_D = 2.2K\Omega$, $R_G = 1M\Omega$, $R_S = 1K\Omega$, $I_{DSS} = 8mA$, $V_P = -4$ Volts. Determine the following parameters: i) V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_G vi) V_D **(10 Marks)**

OR

10 a. With neat sketches, explain the operation and characteristics of n-channel depletion type MOSFET. **(10 Marks)**

b. Derive expression for V_{GS}, I_D, V_{DS}, V_D and V_S for a voltage divider bias circuit using FET. **(10 Marks)**

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