CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive an expression for S_{Ico} and S_{VB} of collector to base bias circuit. **(08 Marks)**

b. Design a suitable Clipper circuit to the output shown in Fig Q1(b). Assume silicon diode.

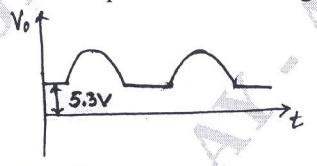

Fig Q1(b) **(05 Marks)**

c. Find I_c, V_E, V_B, V_C and V_{CE} for the circuit shown in Fig 1(c). Assume silicon transistor with $\beta = 60$.

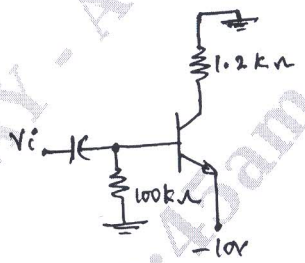

Fig Q1(c) **(07 Marks)**

OR

2 a. Explain how a transistor can be used as a switch. **(07 Marks)**

b. Determine I_E, I_B, V_{CE}, V_{CB}, V_C, and V_E for the network shown in Fig Q2(b). Assume silicon transistor with $\beta = 60$.

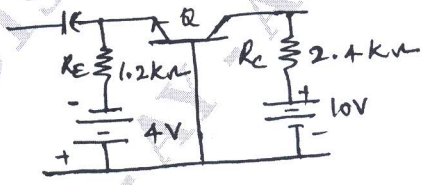

Fig Q2(b) **(07 Marks)**

c. Determine V_o for the network shown in Fig Q2(c) the frequency of i/p signal is 1KHz. Assume ideal diode.

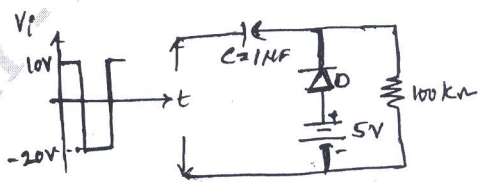

Fig Q2(c) **(06 Marks)**

Module-2

3 a. For the network shown in Fig Q3(a) determine z_i, z_o, A_v and A_I

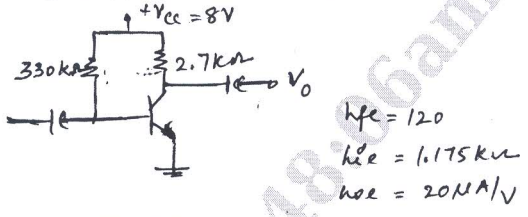

Fig Q3(a) **(08 Marks)**

b. Derive an expression for z_i, z_o, A_v for emitter follower configuration using approximate hybrid model. **(08 Marks)**

c. Obtain the expression for Miller i/p capacitance. **(04 Marks)**

OR

4 a. Draw the complete hybrid equivalent model of a transistor. Derive an expression for z_i, z_o, A_I and A_v. **(10 Marks)**

b. For the common base amplifier shown in Fig Q4(b), determine: i) z_i ii) A_I iii) A_V. Give hie = 1.6kΩ, hfe = 110, hre = 2×10^{-4}, hoe = 20μA/v.

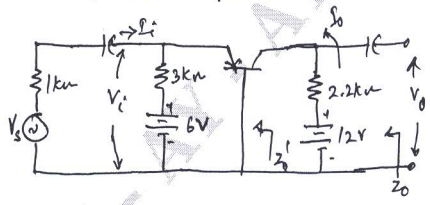

Fig Q4(b) **(10 Marks)**

Module-3

5 a. For the Darlington emitter, follower shown in Fig Q5(a)

i) Calculate the dc bias voltages V_B, V_E, V_c and currents I_B and I_C

ii) Calculate the i/p and o/p impedances

iii) Determine the voltage and current gains

iv) The ac o/p voltage for V_i = 120mV.

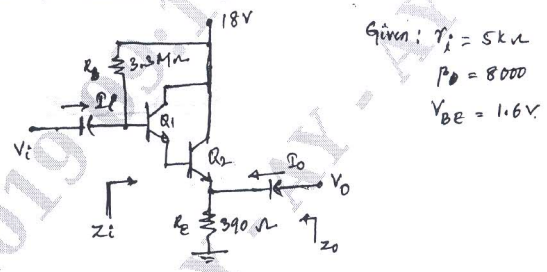

Fig Q5(a) **(10 Marks)**

b. For the cascaded arrangement shown in Fig Q5(b), calculate :

i) The loaded voltage gain of each stage

ii) The total gain of the system A_V and A_{VI}

iii) The loaded current gain of each stage

iv) The total current gain of the system.

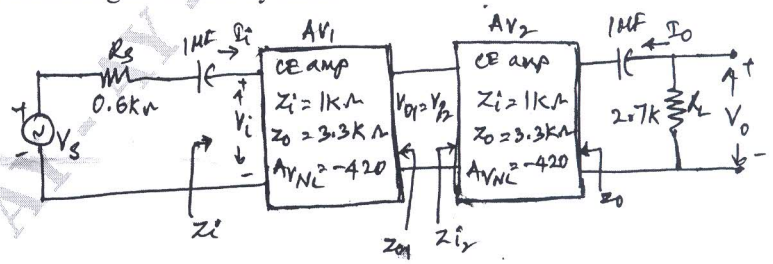

Fig Q5(b) **(10 Marks)**

OR

6 a. List the advantages of negative feedback. **(10 Marks)**

b. Derive an expression for input resistance of current series and current shunt feedback amplifier. **(04 Marks)**

c. Negative feedback to be used to reduce noise from an amplifier by 90% i) what mast the percentage negative feedback to accomplish this, if the initial voltage gain is 50?
ii) What will be the voltage gain with feedback. **(06 Marks)**

Module-4

7 a. Derive an expression for frequency of oscillation of RC phase shift oscillator. **(10 Marks)**

b. With a neat circuit diagram, explain the working of complementary class B power amplifier. **(06 Marks)**

c. The following distortion readings are available for a power amplifier. $D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$ with $I_1 = 3.3$ A and $R_C = 4\Omega$.
i) Calculate THD ii) Determine the fundamental power iii) calculate the total power **(04 Marks)**

OR

8 a. With a neat circuit diagram, explain the working of Hartley oscillator. **(06 Marks)**

b. For a class B amplifier providing a 20V peak signal to a 16Ω load and a power supply of $V_{CC} = 30V$, determine the i/p power, o/p power and efficiency. **(06 Marks)**

c. Explain the classification of power amplifier based on Q- point. **(08 Marks)**

Module-5

9 a. Draw the circuit a fixed bias JFET amplifier and its equivalent circuit. Hence obtain the expression Z_{in}, Z_0 and A_V. **(10 Marks)**

b. A JFET has device parameter of $g_{mo} = 10m\mho$ and $I_{DSS} = 12mA$. When the device is suitably biased, the drain current was found to be 8mA. Determine : i) V_P ii) g_m iii) V_{GS} **(06 Marks)**

c. Give the comparison of FET over BJT. **(04 Marks)**

OR

10 a. With a neat sketch, explain the construction and working principle of N-channel enhancement type MOSFET and also explain its static drain characteristics. **(10 Marks)**

b. Obtain the expression for trans conductance g_m of JFET. **(04 Marks)**

c. For the voltage divider bias configuration shown in Fig Q10(c). Determine the value of R_s, if $V_D = 12V$ and $V_{GSQ} = -2V$.

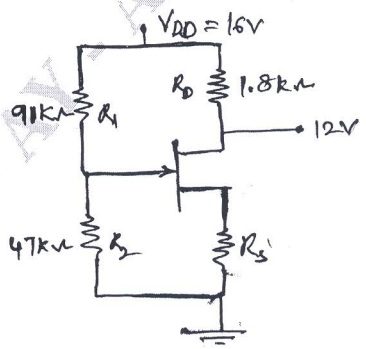

Fig Q10(c) **(06 Marks)**

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