CBCS SCHEME

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15EC655

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With a neat diagram showing the physical structure of an enhancement type NMOS transistor, qualitatively explain the operation of the device under i) no gate voltage ii) positive gate voltage iii) gate voltage and a small voltage between drain and source (No derivations). **(08 Marks)**

b. Given that the permittivity of silicon dioxide is 3.45×10^{-11} F/m, calculate the oxide capacitance if the oxide thickness is 8nm. For a MOSFET device with above specification, if the W/L ratio is 10, threshold voltage is 0.7V and the mobility of electrons is $450cm^2/V.S$, calculate the values of V_{GS} and V_{DS} needed to operate the device in saturation region with a drain current of 100μA. **(08 Marks)**

OR

2 a. With neat circuit diagram, explain the $i_D - v_{DS}$ and $i_D - v_{GS}$ characteristics of enhancement type NMOS transistor. Clearly identify the cut-off, triode and saturation regions, and give the conditions for the same. Also give the current equation in the three regions. **(08 Marks)**

b. With neat circuit diagram and characteristics explain how the MOSFET can be used as i) Switch and ii) as a Linear amplifier. **(08 Marks)**

Module-2

3 a. Explain qualitatively how a resistor between drain and gate terminals results in negative feedback. Design such a circuit to operate at a dc drain current of 0.5mA. Assume $V_{DD} = 5V$, K_n' W/L = $1mA/V^2$, $V_t = 1V$. **(08 Marks)**

b. Using a small signal model for MOSFET, derive the expression for voltage gain of a common source amplifier. **(08 Marks)**

OR

4 a. Derive the expression for input resistance output resistance and voltage gain of common drain configuration. **(08 Marks)**

b. Draw the circuit of capacitively coupled common source amplifier and explain its frequency response, giving reasons for the decrease in the voltage gain at low and high frequency bands. **(08 Marks)**

Module-3

5 a. Compare the characteristics of NMOS and npn transistor amplifiers, with respect to operating conditions, VI characteristics, low and high frequency models, input and output resistances, and intrinsic gain. **(10 Marks)**

b. Show how MOSFET can be used to operate as current source and current mirror. **(06 Marks)**

OR

6 a. Describe the various techniques used for the study and design of IC amplifiers under high frequency conditions. Also derive miller's theorem in high frequency analysis. **(10 Marks)**

b. It is required to design a basic MOSFET constant current source using two transistors Q_1 and Q_2, and one resistor R, to obtain a nominal current output of 100μA. Find the value of R if Q_1 and Q_2 have channel length of 1μm and widths of 10μm, $V_t = 0.7V$, $V_{DD} = 3V$, $I_{ref} = 100\mu A$ and $K_n' = 200\ \mu A/V_2$. **(06 Marks)**

Module-4

7 a. Draw and analyze the circuit of CMOS common source amplifier with active load. Draw the I-V and transfer characteristics, and explain. **(10 Marks)**

b. CMOS common source amplifier with active load has $V_{DD} = 3V$, $V_{tn} = |V_{tp}| = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 65\ \mu A/V^2$, $L = 0.4\mu m$, $W = 4\mu m$, V_{An} 20V, $|V_{AP}| = 10V$, $I_{REF} = 100\mu A$. determine the small signal voltage gain. **(06 Marks)**

OR

8 a. What is meant by cascade connection? Explain the operation of a MOS cascade amplifier. What are its advantages? **(08 Marks)**

What is source degenerated CS amplifier? What are the advantages of source degeneration?

b. Show how the expression derived for the output resistance of a cascode amplifier applies directly to the case of source – degenerated CS amplifier. **(08 Marks)**

Module-5

9 a. Draw the circuit of a basic MOS differential pair configuration, and explain its operation. Show how this circuit rejects common mode voltage. Determine the minimum and maximum limits of common mode voltage that can be applied to the circuit. **(08 Marks)**

b. A MOS differential amplifier is operated at a total current of 0.8mA, using transistor with W/L ratio of 100, $\mu_n C_{ox} = 0.2mA/V^2$, $V_A = 20V$ and $R_D = 5k\Omega$. Find V_{OV}, g_m, r_0 and A_d. **(08 Marks)**

OR

10 a. Draw the circuit of MOS differential pair with current mirror active load, and explain its operation at equilibrium and with differential input signal applied. **(08 Marks)**

b. Draw the circuit of two stage CMOS op-amp and explain its operation. Five the expressions for voltage gains of each stage, and the overall voltage gain. **(08 Marks)**

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