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10EC63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Derive an expression for drain to source current from I-V characteristics for cut-off, triode and saturation regions of MOSFET. **(12 Marks)**

b. For a 0.8μm process technology with aspect ratio 10, t_{ox} = 8nm, $\mu_n = 450 \times 10^8$ $\mu m^2/vs$ and $v_t = 0.7V$

i) Find C_{ox} and K'_n

ii) Calculate the value of V_{GS} and $V_{DS(min)}$ needed to operate the transistor in the saturation region with a dc current $I_D = 100\mu A$.

iii) For the device to operate as 1000Ω resistor, find the values of V_{GS} required for very small V_{DS}. **(08 Marks)**

2 a. Consider a CS amplifier which has g_m = 2MA/V, r_O = 50KΩ, R_D = 10KΩ, R_G = 10MΩ, R_L = 20KΩ and R_{sig} = 500KΩ. Calculate R_{in}, G_v, A_v, A_{v_o} and R_{out}. **(10 Marks)**

b. Explain any three types of biasing methods in MOS amplifier circuits. **(10 Marks)**

3 a. Explain the operation of MOS current steering circuit and mention its advantages. **(10 Marks)**

b. Explain the two different types of scaling process of MOSFET in detail. **(10 Marks)**

4 a. Explain the CMOS implementations of CS amplifiers, also draw its I-V characteristics of active load and determine its small signal voltage gain. **(10 Marks)**

b. Explain the circuit of MOS cascade amplifiers and hence obtain an expression for short circuit transconductance. **(10 Marks)**

PART – B

5 a. Explain the operation of a MOS differential pair with common mode input voltage. **(08 Marks)**

b. Explain the operation of a two stage CMOS Op-Amp configuration. **(06 Marks)**

c. A MOS differential pair operated at a bias current of 0.8mA employs a transistors with W/L = 10 and $\mu_n co_x = K'_n = 0.2mA/v^2$ using R_D = 5KΩ and R_{SS} = 25KΩ. Find the differential gain, the common mode gain and the common mode rejection ratio (in dB) if the output is taken single ended and the circuit is perfectly matched. **(06 Marks)**

6 a. Explain the general structure of feedback amplifiers and also explain the properties of negative feedback. **(08 Marks)**

b. With relevant circuits of series-shunt feedback amplifier, derive the expression for input resistance and output resistance. **(08 Marks)**

c. Explain the effect of feedback on the amplifier poles. **(04 Marks)**

7 a. Draw the sample and hold circuit using Op-Amp and explain it. **(09 Marks)**

b. With neat circuit diagram, explain antilog amplifiers. **(06 Marks)**

c. Design a non-inverting amplifier with a gain of 2 at the maximum output voltage of 10V and the current in the voltage divider to be 10μA. **(05 Marks)**

8 a. Explain the pull-up and pull-down networks used in CMOS logic circuits. **(08 Marks)**

b. Explain the dynamic operation of a CMOS inverter. **(06 Marks)**

c. Implement $F = \overline{AB + CD}$ using AOI. **(06 Marks)**

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