CBCS SCHEME

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17EC53

Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain typical design flow for designing VLSI IC circuit using the flow chart. **(08 Marks)**

b. Write the verilog code for 4-bit ripple carry counter. **(07 Marks)**

c. What are the advantages of HDLs compared to traditional schematic based design? **(05 Marks)**

OR

2 a. Explain top-down design methodology with example. **(08 Marks)**

b. What are the two styles of stimulus application? Explain each method in brief. **(07 Marks)**

c. Mention the features of verilog HDL. **(05 Marks)**

Module-2

3 a. Explain the following verilog data types with an examples,
(i) Nets
(ii) Registers
(iii) Integers
(iv) Parameters
(v) Arrays **(10 Marks)**

b. Write the verilog description of SR-latch. Also write stimulus code. **(06 Marks)**

c. How to write comments in verilog HDL, explain with examples. **(04 Marks)**

OR

4 a. With neat block diagram, explain the components of verilog module. **(08 Marks)**

b. Explain $display, $monitor, $finish and $stop system tasks with examples. **(08 Marks)**

c. Declare the following variables in verilog:
(i) An 8-bit vector net called a_in.
(ii) An integer called count.
(iii) A memory MEM containing 256 words of 64 bits each.
(iv) A parameter cache_size equal to 512. **(04 Marks)**

Module-3

5 a. Write a verilog data flow description for 4-bit full adder with carry lookahead logic. **(08 Marks)**

b. What are rise, fall and turn-off delays? How they are specified in verilog? **(06 Marks)**

c. What would be the output of the following a = 4'b0111, b = 4'b1001

(i) &b (ii) a<<<2 (iii) {a, b} (iv) {2{b}} (v) a ^ b
(vi) a | b **(06 Marks)**

OR

6 a. Write the verilog code for 4-to-1 multiplexer using,
(i) Conditional operator (ii) Logic equation. **(06 Marks)**
b. Discuss And, Or and Not gates with respect to logic symbols, gate instantiation and truth tables. **(08 Marks)**
c. Explain assignment delay, implicit assignment delay and net declaration delay for continuous assignment statements. **(06 Marks)**

Module-4

7 a. Explain the blocking assignment statements and non blocking assignment statements with relevant examples. **(08 Marks)**
b. Write a verilog behavioural description of 8 : 1 multiplexer using case statement. **(06 Marks)**
c. Explain Event based timing control with example. **(06 Marks)**

OR

8 a. Discuss sequential and parallel blocks with examples. **(08 Marks)**
b. Write the verilog behavioural description of 4-bit binary counter. **(06 Marks)**
c. Illustrate the use of while loop and repeat loop with suitable examples. **(06 Marks)**

Module-5

9 a. Explain synthesis process with neat block diagram. **(08 Marks)**
b. Write the structural description of 4-bit equality comparator. **(06 Marks)**
c. Explain the following with general syntax and examples (i) Entity (ii) Architecture. **(06 Marks)**

OR

10 a. Discuss the capabilities of VHDL. **(06 Marks)**
b. Write the VHDL code for two 4-bit comparator using data flow description and when-else statement. **(08 Marks)**
c. Explain the declaration of constants, variables and signals in VHDL with examples. **(06 Marks)**

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