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10ES33

# Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
## Logic Design

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer FIVE full questions, selecting atleast TWO questions from each part.***



### PART – A

1 a. Define canonical minterm forms and canonical maxterm forms. **(04 Marks)**

b. Design a three input, one output minimal two level gate combinational logic circuit which has an output 1 when majority of its inputs are at logic-0 and has an output equal to 0 when majority of its inputs are at logic 1. **(06 Marks)**

c. Use k-map to simplify the following functions :

i) $F(A,B,C,D) = ABD + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}\,B + \overline{A}\,C\,\overline{D} + A\overline{B}\,D$

ii) $F(W,X,Y,Z) = \Sigma_m(1,3,7,11,15) + \Sigma d(0,2,5)$

and realize simplified expressions using Basic Gates. **(10 Marks)**

2 a. Obtain all the prime muplicants of the following Boolean function using Quine – Mocluskey method.

$F(A,B,C,D) = \Sigma_m(1,2,3,5,9,12,14,15) + \Sigma_d(4,8,11)$

And verify the result by using k-map. **(10 Marks)**

b. Simplify the function f(a, b, c, d) = Σm(2, 3, 4, 5, 13, 15) + Σd(8, 9, 10, 11) by using MEV-Map technique and verify the result by using K-map. **(10 Marks)**

3 a. Describe general working principle of Decoder. **(04 Marks)**

b. Implement the following with a suitable decode with active low enable input and active high output

f(w, x, y, z) = Σ (4, 8, 10)

g(a, b, c) = π (1, 3, 6). **(08 Marks)**

c. Draw the interfacing diagram of TEN key, key-pad interface to a digital system using decimal to BCD–encoder. **(08 Marks)**

4 a. Design a 2-bit comparator. **(05 Marks)**

b. Implement the following function using 8 : 1MUX

F(P, Q, R, S) = Σm(0, 1, 3, 4, 8, 15). **(05 Marks)**

c. With a neat logic diagram explain carry look ahead adder. **(10 Marks)**

### PART – B

5 a. Explain how to use SR–latch as a switch de-bounces and draw the relevant timing diagram. **(06 Marks)**

b. Explain the working of master –slave flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

c. How do you convert SR flip-flop to JK flip-flop. **(04 Marks)**

6 a. With the help of a diagram explain the following with respect to shift-registers.
i) Parallel in serial out
ii) Ring counter and twisted ring counter. **(08 Marks)**

b. Design a MOD-6 synchronous counter using JK- flip-flop. **(12 Marks)**

7 a. Draw and explain the block diagram of Mealy and Moore model in a sequential circuit analysis. **(10 Marks)**

b. Realize the system represented by the state diagram shown in Fig.Q7(b) using D-Flip-flop. **(10 Marks)**

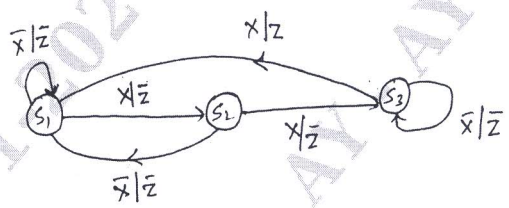


Fig.Q7(b)

8 a. Design a counter using JK flip-flop whose counting is 000, 001, 100, 110, 111, 101, 000 etc by obtaining its minimal sum equations. **(08 Marks)**

b. Construct the excitation table, transition table state table and state diagram for the sequential circuit shown in Fig.Q8(b) below. **(12 Marks)**

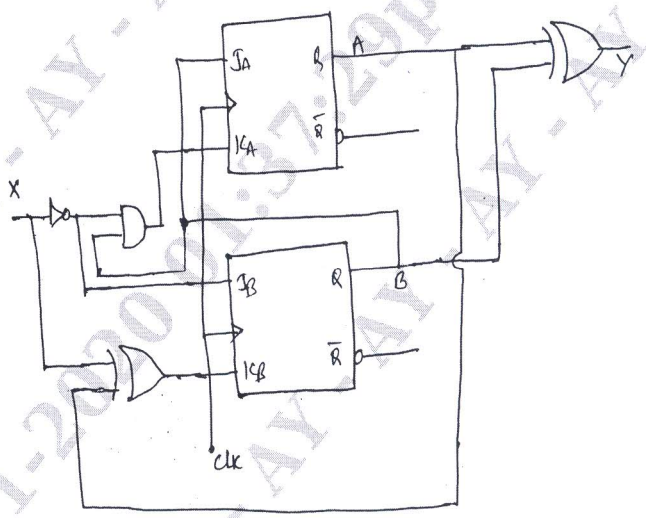


Fig.Q8(b)

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