CBCS SCHEME

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15CS32

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the construction and principles of operation of JFET. **(08 Marks)**

b. Explain with neat sketches, the operation and parameter of n-channel depletion type MOSFET. **(08 Marks)**

OR

2 a. Discuss characteristics of an ideal op-amp and compare with practical op-amp. **(08 Marks)**

b. For the circuit shown in Fig.Q2(b) determine the valve of drain source voltage (V_{DS}). Assume $V_{GS} = -0.8V$.

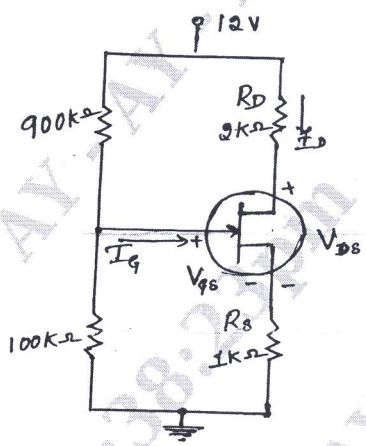


Fig.Q2(b) **(08 Marks)**

Module-2

3 a. What are universal gates? Draw the logic circuit for $y = (A+B+C)(A+B+C)$ using universal gates. **(05 Marks)**

b. Find the minimal SOP of the following Boolean function using K-Map.
F(a, b, c, d) = ∑m(7, 9, 10, 11, 12, 13, 14, 15) **(05 Marks)**

c. Define Hazards? How to design a static 1 hazard free circuit? Explain with an example. **(06 Marks)**

OR

4 a. Simplify the expression y = f(A, B, C, D) = ∑m (1, 2, 8, 9, 10, 12, 13, 14) using Quine – McClusky Method. **(10 Marks)**

b. What is the need of HDL? Write the verilog code for the circuit. Shown in Fig.Q4(b)

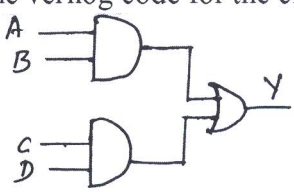


Fig.Q4(b) **(06 Marks)**

Module-3

5 a. What is multiplexer? Write the logic circuit and truth table of 4:1 multiplexer. **(05 Marks)**

b. Explain BCD to Decimal decoder along with circuit diagram. **(05 Marks)**

c. What is magnitude comparator? Design and explain 1 bit magnitude comparator. **(06 Marks)**

OR

6 a. Implement the following function using PLA
$A(x, y, z) = \sum m(1, 2, 4, 6)$
$B(x, y, z) = \sum m(0, 1, 6, 7)$
$C(x, y, z) = \sum m(2, 6)$ **(06 Marks)**

b. Implement the Boolean function expressed by
SOP $f(a, b, c, d) = \sum m(1, 3, 4, 5, 9, 11, 12)$ using 8:1 MUX. **(06 Marks)**

c. Write a note on parity Checker. **(04 Marks)**

Module-4

7 a. What is flip flop? Explain the working of JK master slave flip flop using NAND gates. **(08 Marks)**

b. Write the Execution table of SR, D, JK and T flip flop. **(04 Marks)**

c. Write the difference between synchronous and Asynchronous counter. **(04 Marks)**

OR

8 a. Using Positive edge triggered D flip flop, draw the logic diagram of 4bit SISO Register. Draw the timing diagram to shift binary number 1110 into Register. **(05 Marks)**

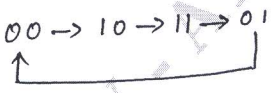
b. Explain with neat diagram 4 bit switched tail counter **(05 Marks)**

c. Explain how shift Register can be applied for sequence detector. **(06 Marks)**

Module-5

9 a. Explain a 3 bit binary Rippledown counter. Give block diagram, truth table and output waveforms. **(08 Marks)**

b. Design a sequences, a module – 4 Irregular counter with following counting sequence using D flip flop. **(08 Marks)**



OR

10 a. Explain 4 bit D/A converter. **(10 Marks)**

b. What is binary ladder? Explain the binary ladder with digital input of 1000. **(06 Marks)**

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