



**Third Semester B.E. Degree Examination, June/July 2019**  
**Analog and Digital Electronics**

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

**Module-1**

- 1 a. Analyze the working of first order high pass filter and also evaluate the expression for gain. Design first order high pass filter at a cut off frequency of 1KHz with pass band gain of 2. And using frequency scaling technique convert 1KHz to 1.6 KHz. (12 Marks)
- b. With the neat sketch explain the working principle of narrow band reject filter with necessary waveforms. (08 Marks)

**OR**

- 2 a. Analyze the working of ALL PASS filter with neat circuit and necessary waveform and also derive the expression for gain. Also find the phase angle if  $F = 1\text{KHz}$ ,  $R = 1.59\text{k}\Omega$  and  $C = 0.01\mu\text{F}$ . (12 Marks)
- b. List the design steps for second order low pass filter. Also design a second order low pass filter at a high cut off frequency of 1KHz. (08 Marks)

**Module-2**

- 3 a. With a neat block diagram analyze the oscillator circuit and also derive the condition for oscillations. (06 Marks)
- b. Analyze the working of a inverting comparator as a Schmitt trigger Also design a Schmitt triggers circuit with  $UTP = +3\text{V}$  and  $LTP = -3\text{V}$ . Draw its input output and hysteresis curve. (14 Marks)

**OR**

- 4 a. With a neat circuit explain working principle of RC phase shift oscillator with necessary equations. Also design a RC phase shift oscillator to have  $F_0 = 200\text{Hz}$ . (12 Marks)
- b. Analyze the working of Non inverting comparator circuit with necessary waveforms. (08 Marks)

**Module-3**

- 5 a. Analyze the working of a 555 timer as monostable multivibrator with neat block diagram as well as circuit diagram. (14 Marks)
- b. The monostable multivibrator is to be used as divide by 2 networks. The frequency of the input trigger signal is 2KHz. If the value of  $c = 0.01\mu\text{F}$ . what should be the value of resistance R. (06 Marks)

**OR**

- 6 a. Explain the operation of 555 timer as Astable multivibrator. (12 Marks)
- b. Analyze the operation of Astable multivibrator as free running ramp generator. (08 Marks)

**Module-4**

- 7 a. Simplify the boolean function  $F(W, X, Y, Z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$  using i) SOP ii) POS form and also write the circuit. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- b. Design a full adder from two half adder. (06 Marks)  
c. Design a 4\*16 decoder circuit using 3\*8 decoder. (04 Marks)

OR

- 8 a. Define MUX. Design  $4 \times 1$  MUX using logic gates Also implement the function  $F(a, b, c) = \Sigma(1, 3, 5, 6)$  using MUX. (10 Marks)  
b. Design BCD to Decimal decoder circuit. (10 Marks)

Module-5

- 9 a. With neat circuit analyze the operation of clocked JK Flip Flop. Also derive the characteristic equation from truth table. (10 Marks)  
b. Design a synchronous 3 bit binary upcounter using the excitation table. (10 Marks)

OR

- 10 a. Design BCD Ripple counter. (10 Marks)  
b. With a neat circuit analyze the operation of clocked SR flip flop using NOR latch. Also derive the characteristic equation from truth table. (10 Marks)

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