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10CS74

Seventh Semester B.E. Degree Examination, June/July 2019
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Define instruction set architecture. Illustrate seven dimensions of ISA. **(08 Marks)**

b. Find the number of dies 350 mm wafer for a die that is 17.5mm on a side and find yield by assuming density of 0.5/cm^2 and manufacturing complexity is 4. **(04 Marks)**

c. Explain the methods and observations to improve the performance of a system. **(08 Marks)**

2 a. With data path explain classic five stage pipeline for a RISC processor. **(06 Marks)**

b. Explain the methods to reduce pipeline branch penalties. **(06 Marks)**

c. List types of exceptions and explain requirements on exceptions. **(08 Marks)**

3 a. Define true data dependences and name data dependences. Explain all possible data hazards. **(07 Marks)**

b. Explain 2-bit branch prediction scheme with state diagram. **(05 Marks)**

c. With neat diagram, explain Tomasulo's approach for dynamic scheduling. **(08 Marks)**

4 a. List the falvours of multiple issue processor with basic VLIW approach. **(08 Marks)**

b. Illustrate how branch target buffer helps in reducing the branch penalties. **(06 Marks)**

c. Explain how speculation supports for register renaming. **(06 Marks)**

PART – B

5 a. Explain Flynn's classification of computers. **(06 Marks)**

b. To achieve a speedup of 80 with 100 processor. What fractions of the original computation can be sequential? **(04 Marks)**

c. Explain directory based cache-coherence protocol. **(06 Marks)**

d. Write a note on memory consistency. **(04 Marks)**

6 a. Derive the CPU execution time equation by considering memory stall cycles. **(05 Marks)**

b. Explain write strategy in first-level of the memory hierarchy. **(05 Marks)**

c. Explain how multilevel cache helps in reducing miss penalty. For 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle and there are 1.5 memory references per instruction what is the average memory access time and average stall cycles per instruction? **(10 Marks)**

7 a. Write the typical multilevel memory hierarchical structure and define 3 C's of misses. **(06 Marks)**

b. Explain compiler optimization with example. **(06 Marks)**

c. Give the differences between SRAM and DRAM. **(03 Marks)**

d. Explain protection via virtual machines. **(05 Marks)**

8 a. Consider a loop for (i = 1; i < = 100; i++)

```
{
  A [i] = A[i] + B[i]; /*S1*/
  B [i + 1] = C [i] + D [i];} /*S2*/
```

What are the dependences between S1 and S2? Is the loop parallel? If not show how to make it parallel? **(06 Marks)**

b. List the drawbacks of dependences. **(04 Marks)**

c. Explain software pipelining with loop unrolling. **(10 Marks)**

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