2002 SCHEME

USN | | | | | | | | | | |

CS33

Third Semester B.E. Degree Examination, June/July 2019

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Verify the following Boolean manipulations and justify each step with respect to postulate or theorem:
i) $abc + ab\bar{c} + a\bar{b}c + \bar{a}bc = ab + ac + bc$
ii) $(ab + c + d)(\bar{c} + d)(\bar{c} + d + e) = ab\bar{c} + d$ **(06 Marks)**

b. Express the following Boolean functions by Maxterm canonical formula without first constructing the Truth-Table. $f(x, y, z) = x + \overline{xz}(y + z)$ **(04 Marks)**

c. Realize 4-bit odd Parity generator using X-OR gates only. **(10 Marks)**

2 a. Using K-maps determine all minimal sums and minimal products for the following Boolean functions. In each case indicate essential Prime Implicants.
$f(w, x, y, z) = \sum m(0, 1, 6, 7, 8, 14, 15)$ **(05 Marks)**

b. Design a combinational network whose input is a 4-bit binary number and whose output is a 2'S complement of input number. **(05 Marks)**

c. For the following Boolean function, determine minimal sums and minimal products using VEM technique, where w, x and y are the map variables and z is map entered variable.
$f = \sum m(2, 3, 5, 12, 14) + dc(0, 4, 8, 10, 11)$ **(10 Marks)**

3 a. Using the Quine-McCluskey method and prime implicant table reductions, determine the minimal sums for the incomplete Boolean function.
$f(v, w, x, y, z) = \sum m(4, 5, 9, 11, 12, 14, 15, 27, 30) + dc(1, 17, 25, 26, 31)$ **(10 Marks)**

b. Explain the procedure for loading a K-map using map entered variable technique. Write the map entered variable K-map for the Boolean function.
$f(w, x, y, z) = \sum m(2, 9, 10, 11, 13, 14, 15)$ **(10 Marks)**

4 a. Explain the operation of a two input TTL NAND-gate with totem-pole output with a neat circuit diagram. **(08 Marks)**

b. What is a FET? Explain how to construct a resistor with the n-channel, enhancement type MOSFET. **(06 Marks)**

c. Explain with the help of a circuit diagram the operation of a two input CMOS nor-gate. **(06 Marks)**

5 a. With a block diagram describe the principle of operation of a carry Look-ahead-adder. **(06 Marks)**

b. What is a Programmable LOGIC Array (PLA)? Describe with a logic diagram the principle of operation of a PLA. What are its advantages? **(08 Marks)**

c. Implement the following Boolean function using 8:1 multiplexer.
$F(A, B, C, D) = \bar{A}B\bar{D} + ACD + \bar{B}CD + \overline{AC}D$ **(06 Marks)**

6 a. What is a sequential circuit? Discuss the different types of sequential circuits. **(06 Marks)**

b. With a neat logic diagram and timing waveforms describe the operation of a master-slave JK flip-flop. **(06 Marks)**

c. A stable assignment table for a mod-5 counter is given below:

S	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1
4	1	1	0

Derive a counter configuration. **(08 Marks)**

7 a. Design a clocked synchronous sequential machine using D-Flip Flops for the following [Fig.Q7(a)] state diagram. Use state reduction if possible. Also draw the logic diagram.

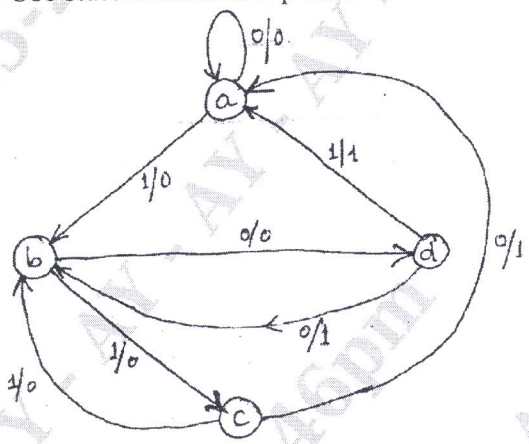

Fig.Q7(a) **(10 Marks)**

b. Design a synchronous Mod-6 counter using T-FF. Write state table and reduce the expression using K-map. Draw the logic diagram. **(10 Marks)**

8 Write short notes on:

a. Implies and subsumes

b. Fan-in and Fan-out

c. Universal shift register

d. Programmable logic arrays **(20 Marks)**

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