MECH 01 / 01

USN | | | | | | | | | | | 10EC45

Fourth Semester B.E. Degree Examination, June/July 2019
Fundamentals of HDL

Time: 3 hrs.   Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Discuss the needs of HDL. Write a brief history of HDL. **(08 Marks)**
b. Discuss HDL data types in detail. **(12 Marks)**

2 a. Write VHDL code for 2 × 1 multiplexer with active low enable using data flow description and assume 7nsec propogation delay for all and , or and not gate. Show the simulation waveforms. **(12 Marks)**
b. With the help of block diagram and Boolean functions, write the verilog data flow description for 3 – bit ripple carry adder. **(08 Marks)**

3 a. Explain sequential statement and its syntax in VHDL and Verilog, with an example. **(10 Marks)**
b. Write VHDL description 4 × 4 bit booth algorithm, with the help of flow diagram. **(10 Marks)**

4 a. Write Verilog structural description for full adder using half adder as component. **(08 Marks)**
b. Write the HDL (VHDL or Verilog) description of an SRAM memory cell. **(12 Marks)**

PART – B

5 a. Write the Verilog description for Fraction binary to Real conversion using task. **(08 Marks)**
b. Write VHDL description using functions to find greatest of two signed numbers. **(08 Marks)**
c. Give the comparison between procedure, task and function. **(04 Marks)**

6 a. Why mixed type description needed? **(04 Marks)**
b. Write mixed type VHDL description for Addition of 5 × 5 matrix. **(12 Marks)**
c. Discuss VHDL package, with an example. **(04 Marks)**

7 a. Highlight the facts of mixed language description. **(06 Marks)**
b. How to invoke a Verilog module from a VHDL module? **(08 Marks)**
c. Discuss the limitations of Mixed Language description. **(06 Marks)**

8 a. What is Synthesis? With a neat diagram, explain the steps involved in a Synthesis process. **(10 Marks)**
b. Explain the mapping of logical operations, with the help of gate level logic diagram. **(10 Marks)**

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