

CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, June/July 2019 Analog Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1. a. Draw the graphical symbol and r_e -equivalent circuit for the common Emitter and common base configuration including the effect of r_o . (06 Marks)
- b. Write the expression for Z_i , Z_o and A_v of a voltage divider configuration using AC equivalent circuit with r_e model, [with bypassed R_E], for a BJT amplifier. (08 Marks)
- c. For the circuit shown in Fig.Q.1(c), determine Z_i , Z_o and A_v . (06 Marks)

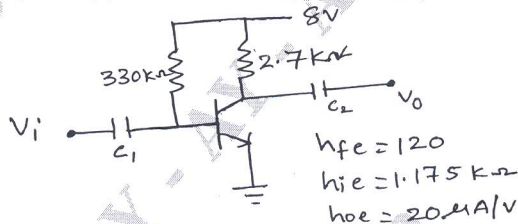


Fig.Q.1(c)

OR

2. a. Draw the circuit diagram of Darlington amplifier and find DC parameters I_{C2} and V_{CE2} . (06 Marks)
- b. Derive the expression for Z_i , Z_o and A_v for common emitter fixed bias configuration using approximate hybrid equivalent circuit. (08 Marks)
- c. Determine input impedance, output impedance and voltage gain of emitter follower, where $V_{CC} = 12V$, $R_B = 220 K\Omega$, $R_E = 3.3 K\Omega$, $\beta = 100$ and $r_o = \infty\Omega$. Use r_e model. (06 Marks)

Module-2

3. a. Describe the construction and working principle of n-channel JFET. (06 Marks)
- b. Derive the expression for Z_i , Z_o and A_v using AC equivalent circuit for JFET common-gate configuration. (08 Marks)
- c. For the FET amplifier show in Fig.Q.3(c). Calculate Z_i , Z_o and A_v with the effect of r_d .

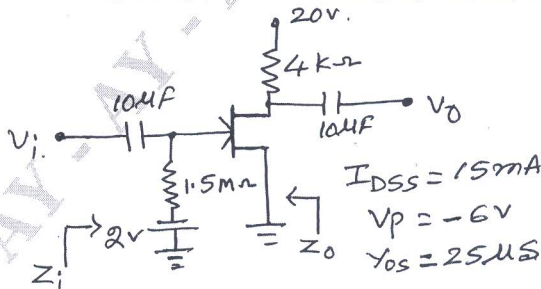


Fig.Q.3(c)

(06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 4 a. Draw and explain the drain and transfer characteristic of n-channel depletion MOSFET. (06 Marks)
- b. Write the ac equivalent circuit for FET self biased configuration and determine Z_i , Z_o and A_v [with R_s bypassed]. (08 Marks)
- c. Give the comparison between JFET and MOSFET. (06 Marks)

Module-3

- 5 a. Draw the single RC coupled BJT amplifier and derive the expression for lower cut-off frequencies due to coupling capacitors C_s and C_c . (10 Marks)
- b. What is miller effect? Prove that Miller effect input capacitance is $C_{mi} = (1 - A_v)C_f$ and out miller effect capacitance is $C_{mo} = \left(1 - \frac{1}{A_v}\right)C_f$. (10 Marks)

OR

- 6 a. Draw the high frequency ac equivalent circuit for FET amplifier and derive f_{Hi} and f_{Ho} . (10 Marks)
- b. Derive the expression for overall higher cut-off frequency for a multistage amplifier. (05 Marks)
- c. An amplifier consists of 3 identical stages in cascade, the bandwidth of overall-amplifier extends from 20Hz to 20kHz. Find the bandwidth of individual stages. (05 Marks)

Module-4

- 7 a. Draw the block diagrams of the following feedback connections types:
i) Voltage-series feedback
ii) Voltage-shunt feedback
iii) Current-series feedback
iv) Current-shunt feedback (08 Marks)
- b. Draw the circuit diagram of FET phase shift oscillator and explain the operation. Write the expression for the frequency of oscillations. (08 Marks)
- c. In a Colpitts oscillator, $C_1 = C_2 = C$ and $L = 100\mu\text{H}$. The frequency of oscillations is 500kHz. Determine the value of C . (04 Marks)

OR

- 8 a. With block diagram of voltage shunt feedback connection type, obtain the expression for input impedance. (08 Marks)
- b. With the help of neat circuit diagram, explain the operation of transistor Hartley oscillator write the expression for the frequency of oscillations. (08 Marks)
- c. A crystal has the following parameter $L = 0.334\text{H}$, $C_m = 1\text{pF}$, $C = 0.065\text{pF}$ and $R = 5.5\text{K}\Omega$. Find the series and parallel resonant frequency. (04 Marks)

Module-5

- 9 a. Explain the operation of series-fed class-A power amplifier and show that maximum conversion efficiency is 25%. (08 Marks)
- b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as $B_0 = 1.5\text{mA}$, $B_1 = 120\text{mA}$, $B_2 = 10\text{mA}$, $B_3 = 4\text{mA}$, $B_4 = 2\text{mA}$ and $B_5 = 1\text{mA}$
i) Determine the percentage total harmonic distortion.
ii) Assume a second identical transistor is used along with a suitable transformer to provide pushpull operation. Use the above harmonic amplitudes to find the new total harmonic distortion. (06 Marks)
- c. Draw the block diagram of shunt voltage regulator and explain the individual blocks. (06 Marks)

OR

- 10 a. What is harmonic distortion? Explain the three point method of calculating the second harmonic distortion. (06 Marks)
- b. A class-B push-pull amplifier operating with $V_{CC} = 25V$ provides a 22V peak signal to an 8Ω load. Find: i) Peak load current ii) dc current drawn from the supply 11P
iii) DC power iv) ac power v) Efficiency. (06 Marks)
- c. Draw the block diagram of series voltage regulator and explain the operation. Also find the o/p voltage and the zener current for the series regulator shown in Fig.Q.10(c). (08 Marks)

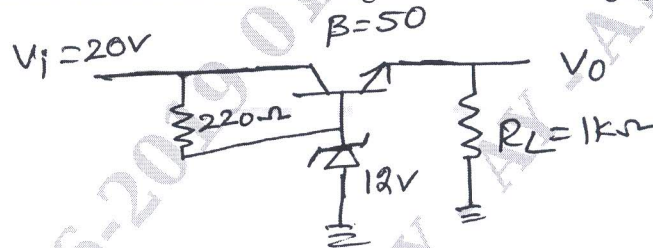


Fig.Q.10(c)
