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Third Semester B.E. Degree Examination, June/July 2019

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Design a combinational logic truth table so that a logic-1 output is generated when majority of four inputs is true (logic-1). Write the canonical minterm and maxterm expressions from truth table in decimal notation. **(04 Marks)**

b. Simplify the following Boolean equations using K-map:
i) $f_1(w, x, y, z) = \Sigma(1, 3, 4, 7, 8, 12) + d(5, 10, 13, 14)$
ii) $f_2(a, b, c, d, e) = \Pi(0, 2, 4, 6, 8, 9, 10, 11, 12, 14, 16, 17, 18, 19, 24, 25, 26, 27)$ **(12 Marks)**

c. What are don't care terms? How are these used by the designer? **(04 Marks)**

2 a. For the Boolean function $f(w, x, y, z) = \Sigma(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$
i) Find the set of prime implicants.
ii) Obtain the minimal SOP expression using Quine-McClusky minimization technique. **(10 Marks)**

b. Simplify the Boolean function $f(w, x, y, z) = \Sigma(2, 9, 10, 11, 13, 14, 15)$ using Variable Entered K-Map (VEM) with variable 'z' as MEV. Realize the simplified expression using NAND gates only. **(10 Marks)**

3 a. With block diagram representation, show how to connect two 74XX138 decoder ICs to form a single 4-to-16 decoder. **(04 Marks)**

b. Realize full subtractor using IC74XX139 and NAND gates. **(06 Marks)**

c. Explain, with diagram, how to use IC74XX147 to interface keypad to a digital system. **(10 Marks)**

4 a. Realize the Boolean function $f(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$ using IC74XX151 (8X1 MUX). Use w, x, y variables for select line inputs. **(05 Marks)**

b. Design 1-bit comparator. **(05 Marks)**

c. Explain, with diagrams, the design of 4-bit adder/subtractor using IC 7483. **(10 Marks)**

PART – B

5 a. Explain SR-latch and $\overline{S}\,\overline{R}$ - latch operation. **(08 Marks)**

b. Explain 0's catching and 1's catching effect in MSJK flip-flop. **(08 Marks)**

c. Explain asynchronous inputs in edge-triggered flip-flops. **(04 Marks)**

6 a. Derive the characteristics equation of JK flip-flop. **(05 Marks)**

b. Draw the logic diagram of parallel-in unidirectional shift register and explain its operation. **(08 Marks)**

c. Explain ring and Johnson counters with diagram and counting sequence. **(07 Marks)**

7 a. Describe the following terms with respect to sequential machines:
i) State ii) Present state iii) Next state **(06 Marks)**

b. For the sequential machine shown in Fig.Q7(b):
i) Write the excitation and output functions
ii) Obtain the transition and state tables.
iii) Draw the state diagram.
iv) Is this a mealy machine or Moore machine?

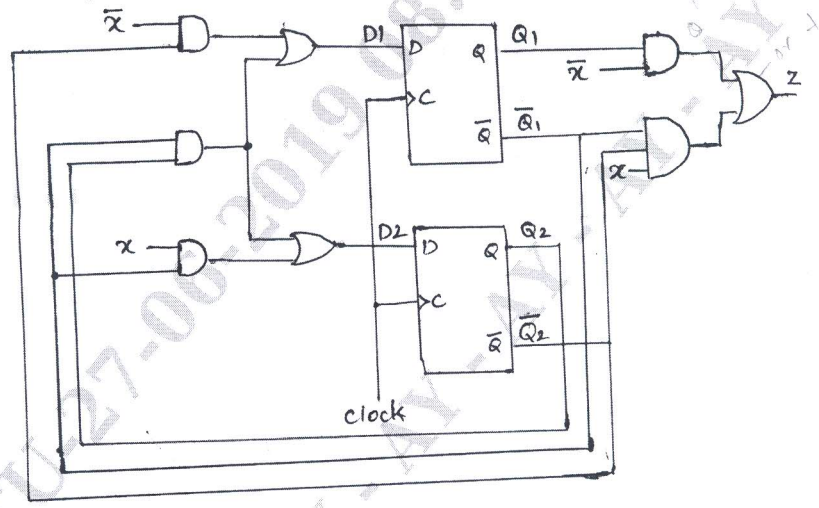

Fig.Q7(b) **(14 Marks)**

8 a. Construct a Mealy state diagram that will detect a serial input sequence 10110. The detection of required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause the output Z to be asserted high. **(08 Marks)**

b. Design a cyclic mod-8 synchronous binary counter using T flip-flops that will count the number of occurrences in an input; that is, the number of times it is a 1. **(12 Marks)**

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