CBCS SCHEME

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17EE46

Fourth Semester B.E. Degree Examination, June/July 2019
Operational Amplifiers and Linear ICs

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define and explain the following terms:
i) Input bias current
ii) Input offset current
iii) CMRR. **(06 Marks)**

b. With a neat circuit diagrams, explain working and design procedure of capacitor coupled voltage follower. **(08 Marks)**

c. For the circuit shown in Fig.Q.1(c), find V_0 given $R_F = 50K\Omega$ and $R_1 = 10K\Omega$ **(06 Marks)**

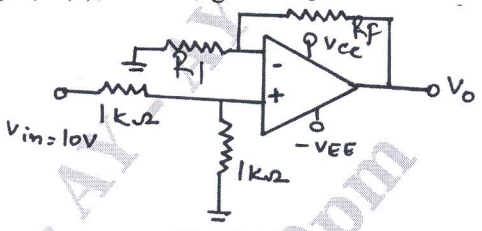

Fig.Q.1(c)

OR

2 a. What is an instrumentation amplifier? Obtain an expression for output voltage V_0, in terms of change in resistance 'ΔR' of an instrumentation amplifier using transducer bridge. **(12 Marks)**

b. Explain with a neat circuit, scaling and averaging amplifier using op-amp in inverting configuration. **(08 Marks)**

Module-2

3 a. Explain the following terms with respect to voltage regulator: i) Line regulation ii) Load regulation iii) Ripple rejection. **(06 Marks)**

b. With a neat circuit diagram, explain working of I order high pass filter and draw its typical frequency response curve. **(10 Marks)**

c. A first order low pass filter has cut off frequency of 1kHz the resistance value designed is 15.6KΩ. Calculate the new value of resistance. If the cut off frequency is to be changed to 1.6kHz. Assume capacitor value as constant. **(04 Marks)**

OR

4 a. Explain working and design of voltage follower regulator. **(07 Marks)**

b. An LM 317 voltage regulator is required to provide 6V output from 15V supply. Load current is 200mA. Design the circuit. Assume $I_1 = 1mA$ $V_{ref} = 1.25V$. **(06 Marks)**

c. Design a wide band pass filter with $f_L = 200Hz$, $f_H = 1kHz$ and pass band gain = 4. Assume capacitor values of high pass and low pass sections as 0.05μF and 0.01μF respectively. Also calculate Q-factor, band width and center frequency. **(07 Marks)**

Module-3

5 a. Explain the working of an inverting voltage comparator circuit. Draw the input, output waveforms when 'V_{ref}' is positive and negative. **(06 Marks)**

b. A triangular/rectangular waveform generator uses μA741 opamp with ±15V supply. Design a suitable circuit to obtain triangular output of $5V_{p-p}$, frequency variation from 200Hz to 2kHz and duty cycle adjustment from 20% to 80% of total time period. **(08 Marks)**

c. With a neat circuit diagram, explain working and design procedure of RC phase shift oscillator. **(06 Marks)**

OR

6 a. With a neat circuit diagram, explain non inverting Schmitt trigger, if UTP is to be made OV, explain the modification to be done in circuit, draw the relevant input/output waveforms. **(10 Marks)**

b. Explain the working of voltage to current converter with grounded load. **(04 Marks)**

c. With a neat circuit diagram, explain Sawtooth ware oscillator. **(06 Marks)**

Module-4

7 a. With a neat circuit diagram, explain working of a non saturation precision half wave rectifier and draw its input and output waveforms. **(08 Marks)**

b. Explain the working principle of linear RAMP analog to digital converter. **(06 Marks)**

c. Design a precision full wave rectifier to produce 2V peak output from sine wave input of peak value 0.5V and frequency of 1MHz, use 741 opamp with ±12V supply. **(06 Marks)**

OR

8 a. Explain R-2R ladder digital to analog converter circuit. **(10 Marks)**

b. Digital input for a 4-bit DAC is 0110. Calculate its analog equivalent output voltage. **(04 Marks)**

c. Explain working ADC using successive approximation method. **(06 Marks)**

Module-5

9 a. With a neat diagram, explain the internal architecture of IC555 timer. **(10 Marks)**

b. Explain the operating principle of phase locked loop. **(06 Marks)**

c. Define the terms related to PLL
   i) Lock range
   ii) Capture range
   iii) Pull in time
   iv) Tracking range. **(04 Marks)**

OR

10 a. Explain how XOR gates can be used as phase detector in PLL. **(06 Marks)**

b. Explain monostable multivibrator, realized using IC555 timer. **(07 Marks)**

c. A PLL system with 105 kHz input has VCO with 100kHz free running frequency and sensitivity of 3.3 kHz/V. Phase detector has sensitivity of 0.68V/rad and amplifier gain of 5. Calculate : i) Loop gain ii) Phase difference iii) Static error voltage iv) Tracking range. **(07 Marks)**

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