CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, June/July 2019
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat circuit diagram, explain Emitter stabilized bias circuit, write the necessary equation. **(08 Marks)**

b. Determine output voltage for the following circuit in Fig.Q.(b). Assume f = 1000Hz and ideal diode. **(06 Marks)**

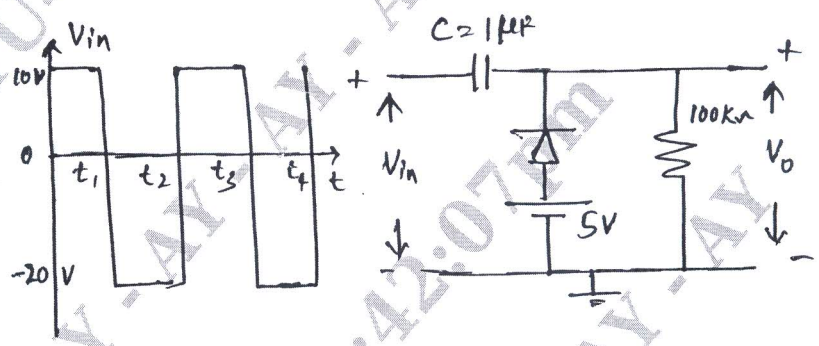

Fig.Q.1(b)

c. Derive the expression for stability factors of fixed bias circuit with respect to I_{CO}, V_{BE}, β and draw the circuit diagram. **(06 Marks)**

OR

2 a. Explain the circuit of a transistor switch being used as an inverter. **(06 Marks)**

b. Determine the voltage V_{CE} and the current I_C for the voltage divider configuration Given: $R_1 = 39K\Omega$, $R_2 = 3.9K\Omega$, $R_C = 10K\Omega$, $R_E = 1.5K\Omega$, $C_E = 50\mu F$, B = 100, $V_{BE} = 0.7$. **(08 Marks)**

c. Sketch the output waveform for the network shown in Fig.Q.2(c). If the peak value of the a.c input if 15V and draw the transfer characteristics. **(06 Marks)**

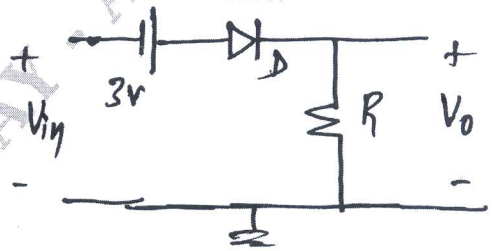

Fig.Q.2(c)

Module-2

3 a. With a neat circuit diagram, derive an expression for Z_i, Z_o and A_v of fixed bias circuit using r_e – model. **(08 Marks)**

b. For the Emitter follower network shown in Fig.Q.3(b). Determine r_e, Z_i, Z_o and A_v. **(06 Marks)**

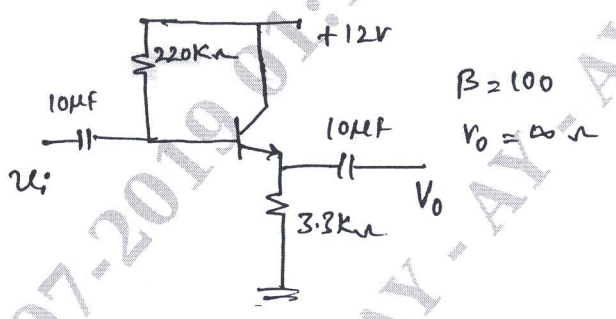

Fig.Q.3(b)

c. Prove that Miller effect of input capacitance $C_{Mi} = (1-A_v)C_f$ and output capacitance $C_{Mo} = \left(1-\frac{1}{A_v}\right)C_f$. **(06 Marks)**

OR

4 a. For the following circuit determine Z_i, Z_o, A_v, A_i $h_{fb} = -0.99$, $h_{ib} = 14.3\Omega$. **(08 Marks)**

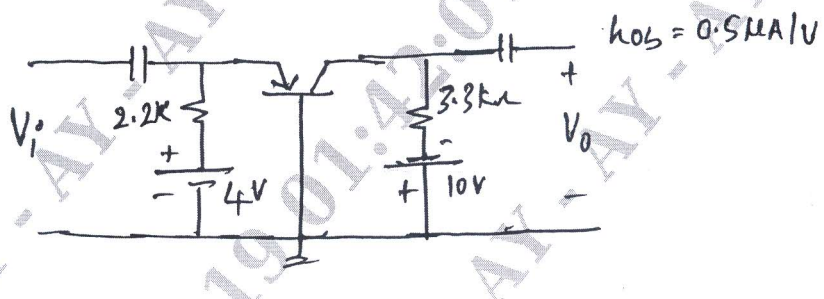

Fig.Q.4(a)

b. What are the advantages of h-parameters? **(06 Marks)**

c. Define h-parameters and obtain h-parameter equivalent circuit of CE configuration. **(06 Marks)**

Module-3

5 a. Obtain expression for voltage gain, current gain, input and output impedance of a Darlington Emitter follower circuit. Draw necessary equivalent circuit. **(12 Marks)**

b. With a neat block diagram, obtain expression for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

OR

6 a. Explain the general characteristics of negative feedback amplifier. **(08 Marks)**

b. Explain the need of cascading amplifier. A given amplifier arrangement has the following gains. $Av_1 = 10$, $Av_2 = 20$ and $Av_3 = 40$. Calculate overall voltage gain and total voltage gain in dB. **(06 Marks)**

c. With a simple block diagram, explain the concept of feedback amplifier. **(06 Marks)**

Module-4

7 a. With a neat circuit diagram, explain the operation of a class B push pull power amplifier and maximum conversion efficiency is 78.5%. **(08 Marks)**

b. With a neat circuit diagram, explain the operation of RC-phase shift oscillator using BJT and write f_{osc} equation. **(06 Marks)**

c. A series fed class A amplifier as shown in Fig.Q.7(c). Operates from a DC source and applied sinusoidal input signal generates peak base current 9mA. Calculate I_{CQ}, V_{CEQ}, P_{dc}, P_{ac} and efficiency. **(06 Marks)**

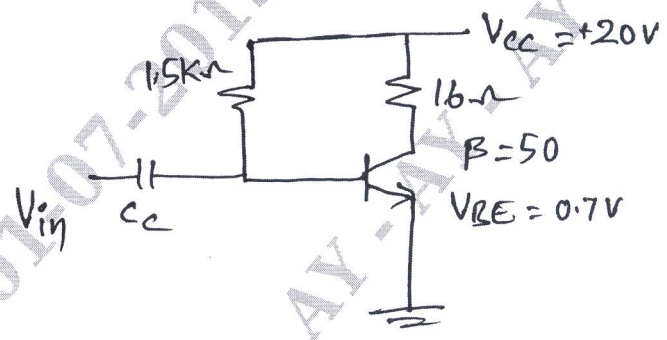

Fig.Q.7(c)

OR

8 a. The frequency selective circuit arms of wein bridge oscillator uses $C_1 = C_2 = 0.001\mu F$, $R_1 = 10K\Omega$ while R_2 is kept variable. The frequency is to be varied from 10Hz to 50kHz by varying R_2. Find the range of R_2. **(06 Marks)**

b. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier and prove that conversion efficiency is 50%. **(08 Marks)**

c. With a neat circuit diagram, explain the working principle of crystal oscillator in series resonant mode. **(06 Marks)**

Module-5

9 a. Explain the operation of JFET amplifier using fixed bias. Draw the JFET small signal model and derive the expression for Z_i, Z_o and A_v. **(06 Marks)**

b. Explain the construction, working and characteristics of n-channel enhancement type MOSFET. **(08 Marks)**

c. Determine the following for network shown in Fig.Q.9(c) V_{GSQ}, V_{DS}, V_S, V_G, V_D. **(06 Marks)**

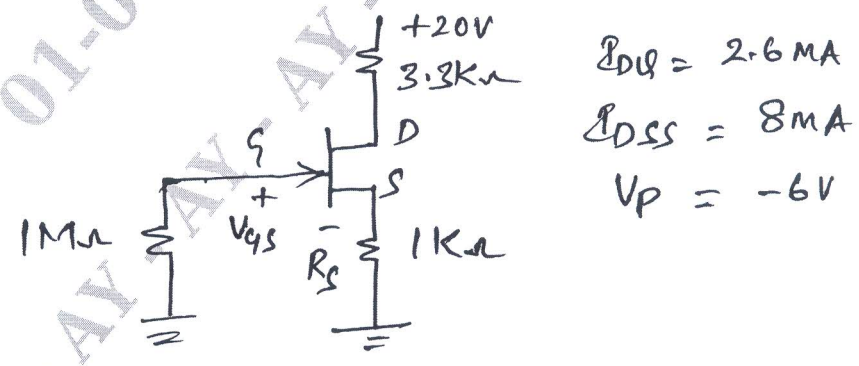

Fig.Q.9(c)

OR

10 a. Compare FET over BJT. **(06 Marks)**

b. With a neat diagrams, Explain the construction, working and characteristics of n-JFET's. **(08 Marks)**

c. Design the fixed bias network as shown in Fig.Q.10(c) having an a.c. gain of 10. Determine the value of R_D. **(06 Marks)**

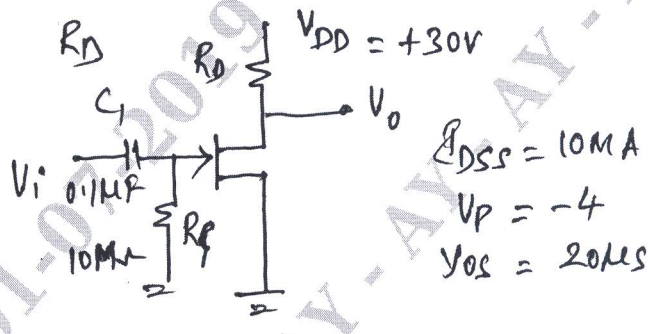

Fig.Q.10(c)

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