

--	--	--	--	--	--	--	--	--	--

Fourth Semester B.E. Degree Examination, June/July 2019
Microprocessors

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1
 - a. With a neat functional block diagram discuss the architecture of 8086 processor. (10 Marks)
 - b. Describe the process of physical address generation in 8086 with an example. (06 Marks)
 - c. Compare and contrast real and protected mode memory addressing. (04 Marks)
- 2
 - a. Define Paging. Draw and discuss the paging mechanism of advanced processors. (10 Marks)
 - b. Define addressing mode. Discuss any five data addressing modes with an example to each. (06 Marks)
 - c. Construct machine code for the following instructions:
(i) MOV BX, CX (ii) MOV DL, [SI + 1240H] (04 Marks)
- 3
 - a. Explain the following instructions with an example:
(i) MUL (ii) XLAT (iii) AAM (iv) CMPSB (v) LOCK (10 Marks)
 - b. Define assembler directives. Explain the following assembler directives with an example.
(i) PUBLIC (ii) ORG (iii) PROC (iv) EQU (10 Marks)
- 4
 - a. Discuss shift instructions with an example. (08 Marks)
 - b. Write an assembly level program to sort an array of N bytes in an ascending order using bubble sort technique. (08 Marks)
 - c. What are the differences between NEAR and FAR procedures. (04 Marks)

PART – B

- 5
 - a. Compare MACRO with procedure. (04 Marks)
 - b. Define Modular programming. Write an algorithm to convert Binary number to ASCII. (08 Marks)
 - c. Develop an assembly level program to read 2 digit Hexadecimal number and display the same on the screen. (08 Marks)
- 6
 - a. What are the functions of the following pins of 8086 processor:
(i) ALE (ii) MN / MX (iii) NMI (iv) QS0, QS1 (v) HOLD (10 Marks)
 - b. Draw and discuss the maximum mode of 8086 processors. (10 Marks)
- 7
 - a. Explain 8086 memory interfacing with an example. (08 Marks)
 - b. Explain absolute address decoding technique with its block diagram. (08 Marks)
 - c. Write differences between I/O mapped I/O and memory mapped I/O. (04 Marks)
- 8
 - a. Describe the architecture of 8255 PPI, with its block diagram. (10 Marks)
 - b. What is IVT? Explain IVT with its structure. (10 Marks)

* * * * *

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.