CBCS SCHEME

USN | | | | | | | | | | |

17CS34

Third Semester B.E. Degree Examination, June/July 2019
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the basic performance equation. Explain the role of each of the parameters in the equation of the performance of the computer. **(04 Marks)**

b. Draw and explain the connections between the processor and the main memory. **(08 Marks)**

c. Write a program to evaluate the arithmetic statement Y = (A + B) * (C + D) using three – address, two-adderss, one–adderss and zero – address instructions. **(08 Marks)**

OR

2 a. What is an addressing mode? Explain any four addressing modes with examples. **(08 Marks)**

b. Explain the concept of stack frames, when subroutines are nested. **(06 Marks)**

c. Explain the shift and rotate operations with examples. **(06 Marks)**

Module-2

3 a. Give comparison between memory mapped I/O and I/O mapped I/O. **(04 Marks)**

b. Explain the following methods of handling interrupts from multiple devices.
i) Interrupt nesting /priority structure
ii) Daisy chain method. **(08 Marks)**

c. What is bus arbitration? Explain distributed arbitration with a neat diagram. **(08 Marks)**

OR

4 a. Draw neat timing diagrams and explain :
i) Multicycle synchronous bus transfer for a read operation.
ii) Asynchronous bus transfer for a write operation. **(12 Marks)**

b. Explain the following with respect to USB.
i) USB architecture
ii) USB addressing. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain the internal organization of a 2M × 8 dynamic memory chip. **(08 Marks)**

b. Distinguish between SRAM and DRAM. **(04 Marks)**

c. Describe any two mapping functions in cache. **(08 Marks)**

OR

6 a. What is virtual memory? With a diagram, explain how virtual memory address is translated? **(08 Marks)**

b. Define the following :
i) Memory latency ii) Memory bandwidth iii) Hit-rate iv) Miss-penalty. **(04 Marks)**

c. Describe the working principle of a typical magnetic disk. **(08 Marks)**

Module-4

7 a. Convert the following pairs of decimal numbers to 5-bit signed 2's complement binary numbers and add them. State whether overflow has occurred.
i) –5 and 7 ii) –10 and –13 iii) –14 and 11. **(06 Marks)**

b. Draw 4-bit carry-look ahead adder and explain. **(06 Marks)**

c. Explain Booth's algorithm, multiply +15 and – 6 using Booth's multiplication. **(08 Marks)**

OR

8 a. Explain the concept of carry-save addition for the multiplication operation M × Q = P for 4-bit operands, with diagram and suitable example. **(08 Marks)**

b. Explain IEEE standard for floating – point numbers. **(06 Marks)**

c. Perform the non-restoring division for 8 ÷ 3 by showing all the steps. **(06 Marks)**

Module-5

9 a. Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction Add R_4, R_5, B_6 for the multiple bus organization. **(10 Marks)**

b. Explain with block diagram the basic organization of a micro programmed control unit. **(10 Marks)**

OR

10 a. With block diagram, explain the working of a microwave oven. **(10 Marks)**

b. Explain the structure of general-purpose multiprocessors with diagrams. **(10 Marks)**

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