10CS33

Third Semester B.E. Degree Examination, June/July 2019
Logic Design

Time: 3 hrs.

Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1 a. With a neat diagram, explain the working of TTL NAND gate. **(06 Marks)**
   b. What are the advantages of HDL? Explain the types of models in HDL with an example of each. **(08 Marks)**
   c. Consider the following logic circuit of Fig.Q1(c). Write the verilog structural code for the same. **(06 Marks)**
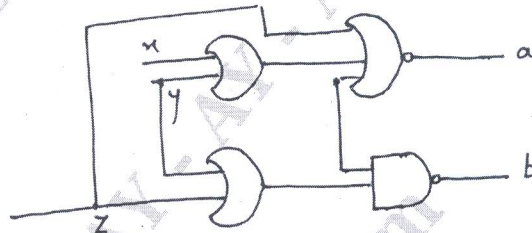

Fig.Q1(c)

2 a. Using K-map, simplify the Boolean expression
   $F(A, B, C, D) = \Sigma m(0, 3, 4, 5, 6, 7, 11, 15) + dc(2, 8, 9, 10, 12, 13)$
   Implement the simplified equation using NAND gates. **(06 Marks)**
   b. For the following K-map of Fig.Q2(b) give SOP and POS form that do not show static 0 or static 1 hazard. **(06 Marks)**

	$\overline{C}$	C
$\overline{A}\,\overline{B}$	1	1
$\overline{A}\,B$	0	0
$A\,B$	1	0
$A\,\overline{B}$	1	0

Fig.Q2(b)

   c. Reduce the following function using Quine McClusky method.
   $F(A, B, C, D) = \Sigma m(1, 4, 6, 8, 9, 10, 11, 12, 13) + dc(3, 15)$
   Implement the simplified equation using NOR Gates. **(08 Marks)**

3 a. Define multiplexer and draw the logic diagram of 4:1 MUX. Implement the Boolean function $F(A, B, C, D) = \Sigma m(1, 7, 9, 10, 12, 13, 14, 15)$ using 8 to 1 MUX. **(06 Marks)**
   b. Draw a ROM circuit that realize the Boolean functions.

   $Y_3 = \overline{A}\,B\,\overline{C}$
   $Y_2 = A\,\overline{B}\,C + ABC$
   $Y_1 = A\,\overline{B}\,C + \overline{A}\,BC + ABC$
   $Y_0 = \overline{A}\,B\,\overline{C} + \overline{A}\,BC + A\,B\,\overline{C} + ABC$ **(07 Marks)**

c. Define an encoder. Design a priority encoder the truth table of which is shown in Fig.Q3(c)
    (07 Marks)

Input				Output	
S	X_1	X_2	X_3	A	B
0	X	X	X	0	0
1	1	X	X	0	1
1	0	1	X	1	0
1	0	0	1	1	1
1	0	0	0	0	0

Fig.Q3(c)

4   a. What is meant by edge triggered flip flop and explain the terms propagation delay, setup
        time and hold time of a flip flop. (04 Marks)
    b. What is excitation table? Write the characteristics equation, state transition diagram and flip-
        flop excitation table for JK flip-flop. Also write the verilog code for SR latch. (07 Marks)
    c. Convert D flip-flop to SR flip flop and draw the logic diagram. (04 Marks)
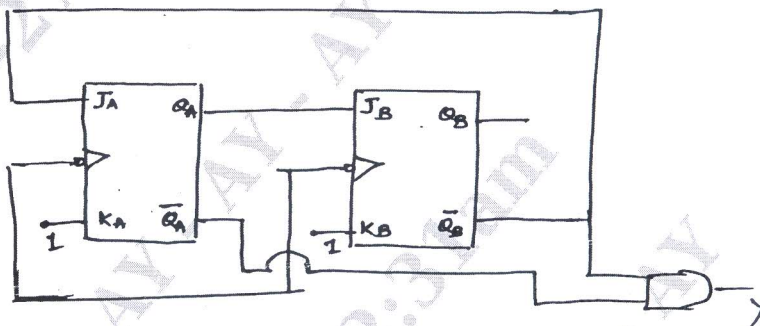   d. Analyse the following circuit of Fig.Q4(d) and indicate what it does. (05 Marks)

Fig.Q4(d)

PART – B

5   a. With a neat diagram, explain 4 bit parallel in serial out shift register using D flip flop.
        (08 Marks)
    b. What is the difference between serial in serial out and parallel in parallel out shift register?
        (02 Marks)
    c. Explain with neat diagram and waveform 4 bit shift register can be used as ring counter and
        Johnson's counter. (08 Marks)
    d. How long will it take to shift an 8 bit number into a 54164 shift register if the clock is set at
        10 MHz. (02 Marks)

6   a. What is modulus of a counter? Design synchronous decade counter using JK flip-flop.
        (08 Marks)
    b. What are decoding gates? What is the primary cause of glitches that occur at the output of a
        decoding gate used with a ripple counter? What is one method to eliminate these glitches?
        (03 Marks)
    c. Define duty cycle. What is the value of duty cycle for an asymmetrical signal if the
        waveform is high for 2 ms and low for 5 ms? (03 Marks)
    d. With a neat diagram and waveform, explain 3 bit asynchronous updown counter. (06 Marks)

7 a. Design a sequence detector using Mealy model that detects three consecutive zero's from an input data stream, x and signals detection by making output, y = 1. **(06 Marks)**
   b. Differentiate between Mealy machine and Moore machine. **(02 Marks)**
   c. Reduce state transition diagram of Fig.Q7(c) by (i) Row elimination method and (ii) Implication table method. **(12 Marks)**
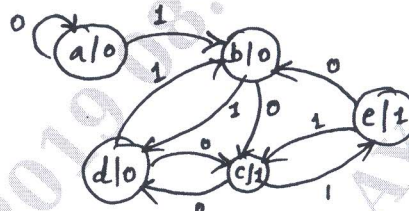

Fig.Q7(c)

8 a. Draw a 4 bit D/A converter using R/2R resistors and explain the working. **(06 Marks)**
   b. What is accuracy and resolution of D/A converter? What is the resolution of a 12 bit D/A converter which uses a binary ladder? If the full scale output is +10V, what is the resolution in volts. **(04 Marks)**
   c. Explain Dual slope A/D conversion. **(10 Marks)**

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