USN | | | | | | | | | | |

10EC63

Sixth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is channel length modulation? Derive the expression for finite output resistance of an NMOS transistor in saturation region. **(08 Marks)**

b. Calculate the value of r_{DS} obtained for a device having $K'_a = 100\,\mu A/V^2$ and W/L = 10 when operated with an overdrive voltage of 0.5V. Assume transistor is opening in triode region. **(04 Marks)**

c. Explain any three Biasing circuits in MOS amplifier. **(08 Marks)**

2 a. From the small signal operation of an amplifier, derive the expression for i) DC bias point ii) Signal current in the drain terminal iii) transconductance and iv) Voltage gain. **(08 Marks)**

b. A transistor amplifier is fed with a signal source having an open circuit voltage V_{sig} of 10mV and an internal resistance R_{sig} of 100kΩ. V_i and V_o are measured both without and with a load resistance R_L = 10kΩ connected to the amplifier output. The measured result are as follows :

	V_i (mv)	V_o (mv)
With R_L	8	70
Without R_L	9	90

Find: i) A_v ii) A_{vo} iii) G_v and iv) G_{vo}. **(04 Marks)**

c. With a neat circuit diagram and small signal model of common drain amplifier prove that $A_{vo} = 1$ and $G_v = 1$. **(08 Marks)**

3 a. For the high frequency equivalent circuit of a common source MOSFET amplifier shown in Fig. Q3(a) having R_{sig} = 100KΩ, R_{in} = 420KΩ, $C_{gs} = C_{gd}$ = 1pF, g_m = 4 MA/V and R'_L = 3.33KΩ. Find the midband voltage gain $A_m = \frac{V_o}{V_{sig}}$ and upper 3dB frequency.

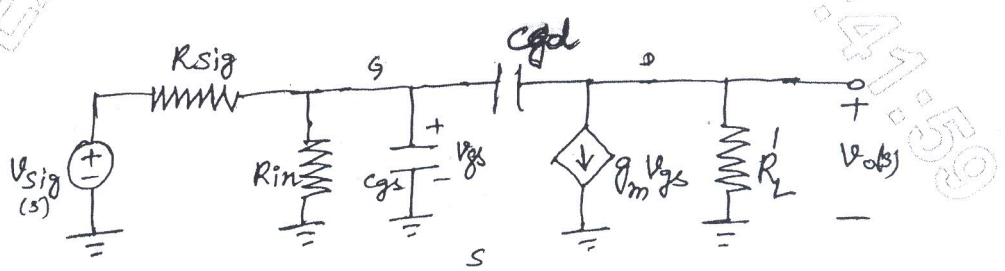

Fig Q3(a) **(08 Marks)**

b. What is scaling of MOSFET? Explain two types of scaling with examples. **(04 Marks)**

c. With a neat circuit diagram, explain the basic MOSFET current source and MOSFET current steering circuit. **(08 Marks)**

4 a. Derive the expression for R_{in}, G_{vo}, A_v and G_v of common gate amplifier with active load. **(10 Marks)**

b. Consider a CC-CE amplifier such that in Fig Q4(b) with the following specifications. $I_1 = I_2 = 1mA$, and identical transistors with $\beta = 100$, $f_T = 400MHz$ and $C_\mu = 2pF$. Let the amplifier be fed with a source V_{sig} having a resistance $R_{sig} = 4K\Omega$ and $r_e = 25m\Omega$. Assume a load resistance of $4K\Omega$, $g_m = 40mA/V$. Find the voltage gain A_m. **(10 Marks)**

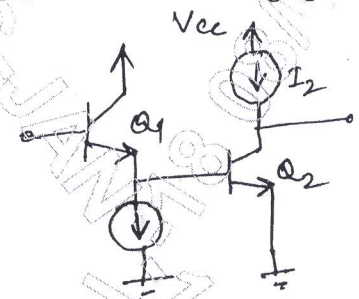

Fig Q 4(b)

PART – B

5 a. Derive the expression for common mode gain common mode rejection ratio of the MOS Differential amplifier. **(10 Marks)**

b. With a neat circuit diagrams explain the working of active loaded MOS Differential pair. **(10 Marks)**

6 a. With a neat block diagram, explain the General structure of feedback. **(08 Marks)**

b. Explain the effect of phase margin on closed loop response and hence prove that $|A_f(jw_1)| = \frac{1.3}{\beta}$. **(04 Marks)**

c. Explain the properties of Negative feedback. **(08 Marks)**

7 a. With neat circuit diagram, explain the working of instrumentation amplifier. **(08 Marks)**

b. Consider the inverting configuration with $R_1 = 1K\Omega$ and $R_2 = 100K\Omega$. Find the closed loop gain for the cases $A = 10^3$ and 10^4. In each case determine the percentage error in the magnitude of G relative to the ideal value of R_2/R_1 (contain with $A = \infty$) Also determine the voltage V_1 that appears at the inverting terminal when $V_i = 0.1V$. **(06 Marks)**

c. With a neat circuit diagram explain the working of antilogarithmic amplifier. **(06 Marks)**

8 a. Explain Digital IC technology and logic circuit families. **(08 Marks)**

b. From the VTC curve, explain the static operation of CMOS invertors. **(06 Marks)**

c. With example explain the working of CMOS logic gate circuit. **(06 Marks)**

* * * * *