CBCS SCHEME

USN | | | | | | | | | | 15MT62

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Embedded System (ARM)

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 Explain the following embedded system hardware components:
i) ARM Bus Technology
ii) ARM Bus protocol
iii) Memory. **(16 Marks)**

OR

2 Describe the following concept:
i) Banked registers
ii) Pipeline instruction sequence
iii) Pipeline executing characteristics. **(16 Marks)**

Module-2

3 a. Explain the following ARM data processing instruction:
i) MOVE instruction
ii) Arithmetic instruction
iii) Comparison instruction. **(08 Marks)**

b. Explain with example for the following instruction:
i) Coprocessor instruction
ii) Coprocessor 15 instruction. **(08 Marks)**

OR

4 Explain the following thumb instruction:
i) ARM-thumb interworking
ii) Branch instruction
iii) Multiple register load store instruction. **(16 Marks)**

Module-3

5 a. What is meant by instruction scheduling and parallel operation preformed in ARM processor. **(08 Marks)**

b. Describe the interlock concept in one cycle interlock caused by load use and delayed load use. **(08 Marks)**

OR

6 Explain the following with example:
i) Allocating variables to register numbers.
ii) Making the most of available registers. **(16 Marks)**

Module-4

7 a. Explain the relationship between the processor core and main memory. **(08 Marks)**

b. With neat diagram describe increasing set associatively. **(08 Marks)**

OR

8 Describe cache policy concept in detail. **(16 Marks)**

Module-5

9 Explain the following exception handling concepts:

i) Vector table **(04 Marks)**

ii) Exception priorities **(06 Marks)**

iii) Link register offsets. **(06 Marks)**

OR

10 a. Explain prioritized simple interrupt handler. **(08 Marks)**

b. Explain nested interrupt handler. **(08 Marks)**

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