CBCS SCHEME

USN | | | | | | | | | | |

17MT36

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw and explain the connection between memory and processor with the respective registers. **(08 Marks)**

b. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. **(05 Marks)**

c. Explain with time line diagram, how the user program and OS routine share the processor for reading a machine level language, data and print the results. Explain how the multitasking can be made possible for the same processor. **(07 Marks)**

OR

2 a. List the different systems used to represent signed numbers perform the following operations on a 4 bit signed numbers using 2's complement representation system:
(i) (+2) + (+3) (ii) (+4) + (– 6) (iii) (–7) – (–5) **(06 Marks)**

b. Write a note on byte addressability, big endian and little endian assignment. **(06 Marks)**

c. Mention four types of operations to be performed by instructions in a computer. Explain with basic types of instruction formats to carryout C ← [A] + [B] **(08 Marks)**

Module-2

3 a. Define an addressing mode. Explain any four addressing mode with an example. **(10 Marks)**

b. Explain the assembler directive concept with neat diagram. **(10 Marks)**

OR

4 a. What is subroutine linkage? With example explain different ways of passing parameters to subroutines. **(10 Marks)**

b. Define stack. Write assembly instruction for safe push operation. **(05 Marks)**

c. Explain logical and arithmetic shift instruction. **(05 Marks)**

Module-3

5 a. Define memory mapped I/O and I/O mapped I/O with example. **(06 Marks)**

b. What is an interrupt? List the sequence of events involved in handling an interrupt request from a single device. **(04 Marks)**

c. Explain the DMA concept in detail. **(10 Marks)**

OR

6 a. Define Bus arbitration. Explain two approaches of bus arbitration. **(12 Marks)**

b. Explain architecture and protocols with respect to USB. **(08 Marks)**

Module-4

7 a. Write a CMOS memory cell and explain the write and read operation of the cell. **(08 Marks)**

b. Discuss the internal organization of a 2M×8 asynchronous DRAM chip. **(08 Marks)**

c. Explain types of read only memory with short description. **(04 Marks)**

OR

8 a. Define cache. With a neat block diagram explain the direct and associative mapping between cache and main memory. **(10 Marks)**

b. What is virtual memory? With neat diagram explain how virtual memory address is translated. **(10 Marks)**

Module-5

9 a. Write control sequence for execution of the instruction Add(R_3), R_1. **(10 Marks)**

b. Explain branching instruction concept with instruction. **(10 Marks)**

OR

10 a. Draw and explain multiple bus organization. **(10 Marks)**

b. With a neat block diagram, explain hardwired control unit show the generation Zin and End control signal. **(10 Marks)**

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