CBCS SCHEME

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15MT35

Third Semester B.E. Degree Examination, June/July 2018
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. With a neat circuit diagram analyze the working of a half wave rectifier with C filter and also derive the expression for the ripple factor. **(07 Marks)**

b. For the full wave 2 diode rectifier circuit with V_i = 10 V(rms), R_s = 0.2 Ω, R_L = 10 Ω, V_D = 0.7V find (i) Peak load current (ii) DC load current (iii) Individual diode dc current (iv) DC output voltage. **(04 Marks)**

c. Design a DC restorer circuit to get the following output waveform with the given input. [Refer Fig.Q1(c)]. **(05 Marks)**

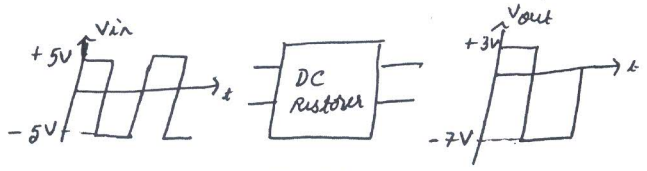

Fig.Q1(c)

OR

2 a. Define the following terms: (i) Reverse Recovery Time (ii) Transition capacitance (iii) Large Signal model. **(09 Marks)**

b. Analyze the working of a zener diode as a voltage regulator and also derive the expression for load voltage. **(07 Marks)**

Module-2

3 a. Analyze the working of a first order low pass Butterworth filter with a neat sketch and frequency response. Also show that $\frac{V_o}{V_{in}} = \frac{AF}{1 + j(f/fH)}$. **(10 Marks)**

b. Design a RC phase shift oscillator for f_o = 200 Hz. **(06 Marks)**

OR

4 a. Design a wide band pass filter with f_L = 200 Hz and f_H = 1 kHz and a pass band gain = 4. Also plot the frequency response and calculate the value of Quality factor. **(08 Marks)**

b. Analyze the working of a Wien Bridge Oscillator with neat sketch and necessary equations. **(08 Marks)**

Module-3

5 a. With a neat circuit and relevant waveforms analyze inverting comparator as Schmitt trigger. And also design a Schmitt trigger circuit with V_{ut} = +3V and V_{lt} = –3V. With supply voltage of ±15V. If supply voltage is 10V(P – P). Find hysteresis voltage. **(10 Marks)**

b. Design a divide by 2 network using a monostable multivibrator for input trigger signal of 2 kHz and c = 0.1 μF. **(06 Marks)**

OR

6 a. Discuss the working of a Astable multivibrator circuit with neat block and waveforms. **(10 Marks)**

b. With a neat circuit and waveforms analyze the working of a non-inverting comparator circuit. **(06 Marks)**

Module-4

7 a. Explain the advantages of CMOS logic and design NAND gate and NOR gate using CMOS logic. **(08 Marks)**

b. Construct a 3-bit ripple down counter using T flip-flop. Write timing diagram and state diagram. Also mention the drawback of ripple counter. **(08 Marks)**

OR

8 a. Explain the working of a TTL logic family with neat sketch. **(08 Marks)**

b. Design a modulo - 10 ripple up counter. Also write its state diagram. **(08 Marks)**

Module-5

9 a. Implement the following Boolean function using 4:1 MUX $f(a, b, c) = \Sigma m(1, 3, 5, 6)$ **(06 Marks)**

b. Explain the working principle of successive approximation type ADC. **(10 Marks)**

OR

10 a. Define decoder construct a circuit for 2 to 4 line decoder. Also implement 3 to 8 line decoder using 2 to 4 line decoder. **(10 Marks)**

b. Explain the operation of R-2R ladder type DAC. **(06 Marks)**

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