CBCS (	Scheme
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USN	95MT36

## Third Semester B.E. Degree Examination, Dec.2017/Jan.2018 Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer FIVE full questions, choosing one full question from each module.

Module-1

- a. Draw and explain the connection between memory and processor with the respective registers. (08 Marks)
  - b. Explain in brief different types of key parameters that affect the processor performance.

(05 Marks)

c. Write different types of computers with short description.

(03 Marks)

OR

- 2 a. List the different systems used to represent signed numbers. Perform the following operations on a 5 bit signed numbers using 2's complement representation system.
  - (i) (+5)+(+10)
  - (ii) (-14)+(+11)
  - (iii) (-3) + (-8)
  - (iv) (-5)-(+7)

(05 Marks)

- b. Write a program that can evaluate the expression  $A \times B + C \times D$  in a single accumulator processor. Assume that the processor has Load, Store, Multiply and add instruction and that all values fit in the accumulator.

  (03 Marks)
- c. Mention four types of operations to be performed by instructions in a computer. Explain with basic types of instruction formats to carryout C [A]+[B] (08 Marks)

Module-2

- 3 a. Define an addressing mode. Explain the following addressing modes with example:
  - (i) Immediate
  - (ii) Indirect
  - (iii) Index
  - (iv) Relative
  - (v) Auto increment and auto decrement.

(10 Marks)

b. There are n = 100 numbers stored in the memory location starting from NUM 1 at 208. Each of the numbers is word organized. It is required to add these numbers and store at memory location SUM. Write an assembly language program to perform this task. Use the necessary assembler directives.

OR

- 4 a. Registers R5 is used in a program to point to the top of a stack. Write a sequence of instruction using the index, auto increment and auto decrement addressing modes to perform each of the following tasks:
  - (i) POP the top two items off the stack, add them and then push the result onto the stack.
  - (ii) COPY the fifth item from the top into register R<sub>8</sub>.
  - (iii) Remove the top ten items from the stack.

(04 Marks)

## 15MT36

Both of the following statements cause the value 300 to be stored in location 1000, but at different times. ORIGIN 1000 DATAWORD 300 and (04 Marks) MOVE # 300, 1000 What is subroutine linkage? With example explain different ways of passing parameters to (08 Marks) subroutines. Module-3 Define memory mapped I/O and I/O mapped I/O with example. (04 Marks) Explain how interrupt request from several I/O devices can be communicated to a processor (04 Marks) through a single INTR line. (08 Marks) Describe DMA concept in brief. Define bus arbitration. Explain in detail any one approach of bus arbitration. (08 Marks) (08 Marks) Discuss briefly the protocols of USB. Module-4 Draw a neat diagram of 16×8 bit organized TR ×1 memory chip. Explain the read and write (06 Marks) operation of the memory. b. Discuss the internal organization of a 2M×8 asynchronous DRAM chip. (07 Marks) Explain with short description any four non-volatile memory concepts. (03 Marks) What is meant by cache? With a neat block diagram, explain the direct and set associative 8 (08 Marks) mapping between cache and main memory. The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger or smaller? (02 Marks) What is virtual memory? With a diagram, explain how virtual memory address is translated. (06 Marks) Module-5 Write the single bus organization of the data paths inside a processor and explain the (10 Marks) importance of each unit. Write and explain the control sequence for execution of an unconditional branch instruction.

OR

(08 Marks) 10 a. Draw and explain multiple bus organization. b. With a neat block diagram, explain hardwired control unit show the generation Zin and End (08 Marks) control signal.