2002 SCHEME

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CS33

Third Semester B.E Degree Examination, June/July 2018
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Using the theorems of Boolean algebra, simplify the following:

i) $y_1 = D(\overline{A} + B) + \overline{B}(C + AD)$

ii) $y_2 = \overline{A\overline{B} + ABC + A(B + A\overline{B})}$

iii) $y_3 = A\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$. **(09 Marks)**

b. Express the following expressions in canonical form:

i) $y_1 = (A + B)(A + C)(B + \overline{C})$

ii) $y_2 = AC + AB + BC$. **(06 Marks)**

c. Give the implementation of EXOR gate using minimum number of NAND gates only. **(05 Marks)**

2 a. i) Express the following min term expression in POS form:
$y(A, B, C, D) = \Sigma m(1, 3, 5, 6, 7, 9, 10, 12, 15)$

ii) Express the following max term expression in SOP form:
$y(A, B, C) = \pi M(0, 3, 5, 6)$. **(06 Marks)**

b. i) What are the advantage, disadvantages of K map?

ii) Simplify the following function in SOP form using K Map:
$f(A, B, C, D) = \overline{A}\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C}$ **(08 Marks)**

c. Simplify the following function in POS form using K map:
$f(A, B, C, D) = \pi M(0, 1, 2, 5, 8, 9, 10)$. **(03 Marks)**

d. Simplify the following function in SOP form using K map:
$y(w, x, y, z) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(03 Marks)**

3 a. Minimize the expression using Quine Mc Cluskey method.
$y(A, B, C, D) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(10 Marks)**

b. Simplify the following using VEM technique. Reduce 4 variables to 3 variables.
$y = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}BC\overline{D} + ABCD + ABC\overline{D}$
(05 Marks)

c. Realize a full adder using minimum number of 2 input NAND gates. Write the truth table, relevant expressions and logic diagram. **(05 Marks)**

4 a. Define: i) Propagation delay ii) Power-delay product iii) Fan-out iv) Noise margin. **(04 Marks)**

b. Write the circuit diagram of a TTL NAND gate and draw and explain the transfer characteristic. **(07 Marks)**

c. Explain with respect to TTL the following output stages:
i) Totem pole ii) Open collector iii) Tri-state output. **(09 Marks)**

5 a. Draw the circuit of a JK-flipflop using NAND gates building blocks. Verify that JK-flipflop satisfy the difference equation: $Q_{n+1} = J_n \overline{Q}_n + \overline{K}_n Q_n$. **(10 Marks)**

b. Show how JK-flipflop can be connected as i) D-flipflop ii) T-flipflop. **(06 Marks)**

c. Describe a C-MOS inverter with relevant circuit diagram. **(04 Marks)**

6 a. Using PROM, realize the following expressions.

$f_1(x_2, x_1, x_0) = \sum m(0, 1, 2, 5, 7)$; $f_2(x_2, x_1, x_0) = \sum m(1, 2, 4, 6)$ **(08 Marks)**

b. Distinguish between PLA and PAL. **(04 Marks)**

c. What is a register? With a neat logic diagram, explain universal shift register. **(08 Marks)**

7 a. Explain gated SR latch using NAND gate. **(06 Marks)**

b. Design a mod – 5 synchronous binary counter using JK flip – flop. **(10 Marks)**

c. Find out characteristic equations of S-R FF and J-k FF. **(04 Marks)**

8 Write short notes on the following :

a. 1 – bit comparator

b. Single decode BCD adder

c. Shannon's Expansion theorem

d. Mod – 8 twisted ring counter. **(20 Marks)**

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