CBCS Scheme

USN			15MT62
Sixth Semester B.E. Degree Examination, June/July 2018			
Embedded System (ARM)			
Tin	ne: 1	3 hrs. Max. M	arks: 80
Note: Answer FIVE full questions, choosing one full question from each module.			
		Module-1	
1	a.	What is meant by ARM? List out steps present in ARM design philosophy.	(06 Marks)
	b.	Describe in short memory and pheripherals concept present in embedded system	hardware.
			(10 Marks)
2		OR	
2	a.	Describe the following:  (i) Generic program status register. (ii) Processor modes.	(Of Maulia)
	b.	Discuss core extensions concept with neat diagram.	(06 Marks) (10 Marks)
	٥.	Module-2	(10 Marks)
3	a.	Explain the following ARM instruction with example,	
		(i) Comparison instruction. (ii) Multiply instruction.	(08 Marks)
	b.	List out addressing mode for load store multiple instructions.	(08 Marks)
		OR	~ (6) ° _
4		Explain the following thumb instruction:	
	a.	Branch instruction.	900
	b.	Software interrupt instruction.  Stack instruction.	(ICM-1-)
	C.	Module-3	(16 Marks)
5	a.	Write one cycle interlock caused by delayed load use with example.	(04 Marks)
	b.	Describe the following Load scheduling process:	(01111111111111111111111111111111111111
		(i) Load scheduling by preloading.	
		(ii) Load scheduling by unrolling.	(12 Marks)
		OR	
6		Explain the following concept in Register. Allocation with example,	
	a.	Using more than 14 local variables.	// C N K . N . N
	b.	Making the most of available registers.  Module-4	(16 Marks)
7	a.	With neat diagram, explain the relationship of cache has between the processor	or core and
,		main memory.	(08 Marks)
	b.	Explain main memory maps to direct mapped cache.	(08 Marks)

Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

8

9 Write following concept with neat description: Assigning interrupts.

Locking a cache using lock bits.

Describe the following concept in cache Lockdown:

Locking a cache by incrementing the way index.

Interrupt latency, b.

IRQ and FIQ exceptions. (16 Marks) OR

OR

Module-5

10 Explain the following:

Nonnested interrupt handler.

Nested interrupt handler. (16 Marks)

(16 Marks)