CBCS SCHEME

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15EC53

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain top-down design methodology with an example. **(06 Marks)**

b. Explain the typical design flow for designing VLSI IC circuits, with a neat flow chart. **(10 Marks)**

OR

2 a. Explain Bottom-up design methodology with an example. **(06 Marks)**

b. Explain the different levels of abstraction used for programming in verilog. **(10 Marks)**

Module-2

3 a. Explain system tasks and compiler directives in verilog. **(06 Marks)**

b. What are the basic components of a module? Explain all the components of a verilog module with a neat block diagram. **(06 Marks)**

c. Write verilog description of SR Latch. Also write stimulus code. **(04 Marks)**

OR

4 a. Write a note on: i) Registers ii) Nets iii) Arrays iv) Parameters v) Vectors vi) Memories. **(12 Marks)**

b. Declare a top-level module "Stimulus". Define Reg_in (4 bit) and Clk (1 bit) as register variables and Reg_out (4 bits) as wire. Instantiate the module "shift-reg" in "stimulus" block and connect the ports by ordered list. Declare A (4 bit) and clock (1 bit) as inputs and B (4 bit) as output in "shift-reg" module. (No need to show internals). Write a verilog code for the above. **(04 Marks)**

Module-3

5 a. Write the verilog description of 4 bit ripple carry adder at gate level abstraction, with a neat block diagram. Also, write stimulus block. **(08 Marks)**

b. What would be the output of the following:
a = 4'b1010, b = 4'b1111
i) a & b ii) a && b iii) & a iv) a >> 1 v) a >>> 1 vi) y = {2{a}}
vii) a ∧ b viii) z = {a, b}. **(08 Marks)**

OR

6 a. A full subtractor has three 1-bit inputs x, y and z (previous borrow) and two 1-bit outputs D(Difference) and B(Borrow). The logic equations are

$D = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$

$B = \bar{x}y + \bar{x}z + yz$

Write verilog description using dataflow modeling. Instantiate the subtractor module inside a stimulus block and test all possible combinations of inputs x, y and z. **(08 Marks)**

b. Design 4:1 multiplexer using gate level modeling or structural description. Write stimulus block. (08 Marks)

Module-4

7 a. Explain structured procedure statements in verilog. (06 Marks)
b. Write a verilog behavioral 8:1 multiplexer program using case statement. (06 Marks)
c. Explain casex and casez statements in verilog. (04 Marks)

OR

8 a. Explain procedural assignment statements in verilog. (06 Marks)
b. Explain sequential and parallel blocks with examples. (06 Marks)
c. Write a verilog code to find the first bit with a value 1 in
Flag = 16′b 0010_0000_0000_0000. (04 Marks)

Module-5

9 a. Explain the design tool flow followed in VLSI design with a neat flow diagram. (10 Marks)
b. Write VHDL Data flow description of 1 Bit full Adder. (06 Marks)

OR

10 a. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL. (10 Marks)
b. Write VHDL structural description of 1 Bit Full Adder. (06 Marks)

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