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10EC56

**Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019**

**Fundamentals of CMOS VLSI**

Time: 3 hrs.

Max. Marks:100

**Note: 1. Answer any FIVE full questions, selecting at least TWO full questions from each part.  
2. Assume missing data, if any.**

**PART – A**

- 1 a. Obtain the transfer characteristics of a CMOS inverter and mark all the regions showing the status of PMOS and NMOS transistors. (08 Marks)
- b. Using neat diagrams, describe fabrication steps of P-well CMOS process. (08 Marks)
- c. Discuss the nMOS enhancement mode transistor for different conditions of  $V_{ds}$  and  $V_{gs}$ . (04 Marks)
- 2 a. Discuss in detail the  $\lambda$ -based design rules for nMOS, and PMOS layers and transistors. (10 Marks)
- b. Illustrate the schematic and stick diagram for the expression  $Y = \overline{A(B + C)}$ . (10 Marks)
- 3 a. Explain the operation of CMOS dynamic logic. Also discuss the cascading problem of dynamic CMOS logic. (10 Marks)
- b. Realize a 3-input NAND gate for clocked CMOS logic and also for CMOS domino logic. (06 Marks)
- c. Discuss the working of pseudo nMOS logic with suitable example. (04 Marks)
- 4 a. What is sheet resistance? Derive the expression for sheet resistance. (06 Marks)
- b. Derive the equation for rise and fall time for CMOS inverter. (08 Marks)
- c. Write a note on limitations of scaling. (06 Marks)

**PART – B**

- 5 a. Discuss the architectural issues of CMOS subsystem design. (04 Marks)
- b. Explain structured design of bus arbitration logic for n-line bus. (10 Marks)
- c. Explain: i) Dynamic register element ii) Dynamic shift register. (06 Marks)
- 6 a. Design 4-bit ALU to implement addition, subtraction, EXOR, EXNOR, OR and AND operations. (10 Marks)
- b. With the neat diagram explain 4-bit serial-parallel multiplier. (10 Marks)
- 7 a. Explain with neat diagram the three transistor dynamic RAM cell. (10 Marks)
- b. Explain nMOS pseudo-static memory cell using circuit and stick diagram. (10 Marks)
- 8 a. Narrate the meaning of "Real Estate" in VLSI design. (05 Marks)
- b. Explain: i) Built-In-Self-Test (BIST) ii) Boundary Scan Test (BST). (10 Marks)
- c. Write a short note on scan design techniques. (05 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.