CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Convert $x = \bar{a}b + bc$ to canonical SOP form. **(02 Marks)**

b. Simplify $G = f(w,x,y,z) = \pi M(1,3,8,10,12,13,14,15)$ in POS form and implement using NOR gates. **(08 Marks)**

c. Simplify the following using Quine-McClusky's minimization technique.
$V = f(a, b, c, d) = \sum m(1, 3, 4, 5, 6, 9, 11, 12, 13, 14)$ **(10 Marks)**

OR

2 a. Convert $P = (\overline{w} + x)(y + \overline{z})$ to canonical POS form. **(03 Marks)**

b. Simplify $P = f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$ in SOP form and implement using NAND gates. **(07 Marks)**

c. Simplify using Quine-McClusky's minimization technique:
$V = f(a, b, c, d) = \sum m(1, 5, 7, 9, 13, 15) + \sum d(8, 10, 11, 14)$ **(10 Marks)**

Module-2

3 a. Implement $f_1(a, b, c) = \sum m(1, 3, 5)$; $f_2(a, b, c) = \sum m(0, 1, 6)$ using 74138, 3:8 decoder. **(06 Marks)**

b. With a neat circuit diagram explain the carry look ahead adder with relevant expressions. **(10 Marks)**

c. Design a one-bit comparator, implement using suitable gates. **(04 Marks)**

OR

4 a. Using 74151, 8:1 Mux, realize the Boolean function $F(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 10, 15)$ with b, c, d as select lines. **(04 Marks)**

b. With neat circuit diagram, explain the keypad interface using 74147, 10 line to BCD encoder. **(10 Marks)**

c. Design a full subtractor and implement using logic gates. **(06 Marks)**

Module-3

5 a. Discuss the working principle of Gated SR latch with its truth Table. **(06 Marks)**

b. Explain the operation of Switch debouncer built using SR latch with the help of circuit and waveforms. **(08 Marks)**

c. Obtain the characteristic equations of JK flip flop and SR flip flop. **(06 Marks)**

OR

6 a. What is race around condition? How it can be overcome? **(02 Marks)**

b. Explain the working of MS-JK flip flop with logic symbol and timing diagram. **(10 Marks)**

c. Explain the working of +ve edge triggered D flip flop with the functional table. **(08 Marks)**

Module-4

7 a. Explain the working of four bit ripple counter using +ve edge triggered T flip-flops with the counting sequence table and timing diagram. **(10 Marks)**

b. Explain the SIPO and SISO operation of shift register with relevant logic diagram and the truth table. **(06 Marks)**

c. Explain the operation of ring counter using logic diagram and truth table. **(04 Marks)**

OR

8 a. Explain Universal Shift Register with the help of logic diagram and mode control table. **(10 Marks)**

b. Realize a three-bit binary synchronous up counter using JK flip flops. **(10 Marks)**

Module-5

9 a. Construct a Mealy state diagram that will detect input sequence 10110, when input pattern is detected Z is asserted high. Write the state diagram. **(10 Marks)**

b. Design a synchronous counter using T flip flops to count the sequence 0, 2, 3, 6, 5, 1, 0, 2, … Write the excitation table and state diagram and logic diagram. **(10 Marks)**

OR

10 a. Explain Mealy and Moore model of clocked synchronous sequential circuit with the block diagram. **(08 Marks)**

b. For the logic diagram given in Fig.Q10(b):

i) Derive the excitation and output equations
ii) Write the state equations
iii) Construct transition table and state table
iv) Draw the state diagram

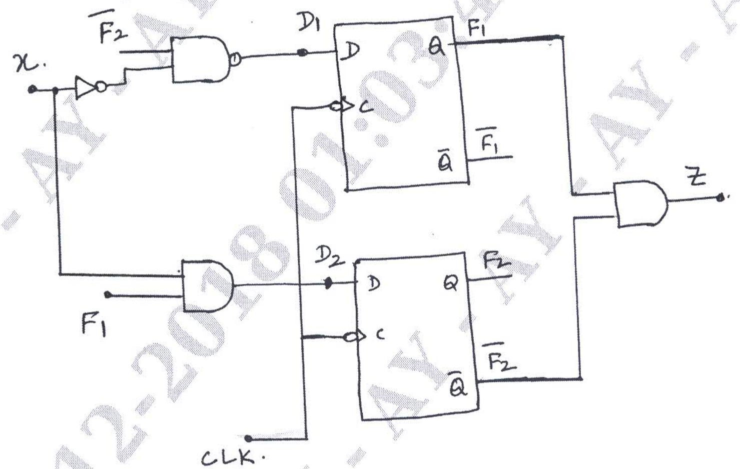

Fig.Q10(b) **(12 Marks)**

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