Third Semester B.E. Degree Examination, Dec.2018/Jan.2019 Digital System Design

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

a. Define a combinational circuit. With block diagram, explain the steps involved in designing the combinational circuit. (06 Marks)

b. Simplify the Boolean function using K-map.

 $F(A, B, C, D) = \sum m(0, 4, 5, 8, 12, 13, 16, 20, 21, 24, 28, 29)$

(06 Marks)

c. Define the following terms:

i) Maxterm

ii) Minterm

iii) Canonical SOP

iv) Canonical POS

(04 Marks)

OR

2 a. Simplify the following function using 3-variable MEV K-map.

 $f(A, B, C, D) = \sum m(0, 1, 3, 5, 6, 11, 13) + d(4, 7)$

(06 Marks)

b. Simplify the given Boolean function using Quine-McCluskey method.

 $f(A, B, C, D) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$

(10 Marks)

Module-2

a. Design a combinational circuit to convert BCD to Excess-3.

(06 Marks)

b. Implement the multiple functions

 $f_1(a, b, c, d) = \sum m(1, 4, 8, 13)$

 $f_2(a, b, c, d) = \sum m(2, 7, 13, 14)$

using two 74138 (3 to 8) decoders.

(06 Marks)

c. Implement a full adder using 4:1 multiplexed.

(04 Marks)

OR

4 a. Define magnitude comparator. Design a 4-bit binary comparator and implement with suitable logic gates. (10 Marks)

b. Implement the following function

 $f(a, b, c, d) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$

using 8:1 multiplexer.

(06 Marks)

Module-3

5 a. Explain with waveforms a switch de-bouncer using SR latch.

(06 Marks)

b. Explain the working of Master-Slave S-K flip-flop with the help of logic diagram, functional table, logic symbol. (06 Marks)

c. Obtain the characteristic equation for J-K and S-R flip-flops.

(04 Marks)

OR

6 a. With a neat logic diagram, explain the working of positive edge triggered D-flip-flop.

(06 Marks)

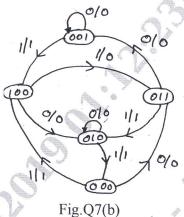
b. Design a synchronous counter to give a counting sequence 0, 2, 3, 6, 5, 1, 0... using J-K F/F. (06 Marks)

c. With the help of a schematic diagram, explain a serial shift register can be transformed into a (i) ring counter (ii) Johnson counter. (04 Marks)

Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice. Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

Module-4

- 7 a. Explain Mealy and Moore models of a clocked synchronous sequential circuits. (06 Marks)
 - b. A sequential circuit has one input and one output state diagram is as shown in Fig.Q7(b). Design the sequential circuit with J-K F/F.



(10 Marks)

OR

8 a. Analyze the sequential circuit shown in Fig.Q8(a). Construct the excitation table, transition table, state table and state diagram for sequential circuit shown in Fig.Q8(a).

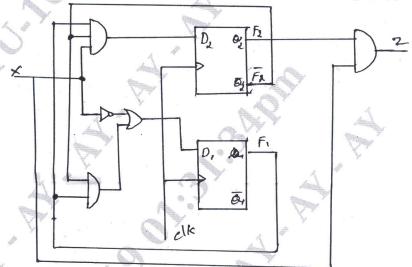


Fig.Q8(a)

(10 Marks)

b. Write the differences between combinational and sequential circuits.

(06 Marks)

Module-5

- 9 a. With general syntax and suitable example, explain the logical and relational operators in VHDL. (06 Marks)
 - b. Explain the various data types available in VHDL.

(10 Marks)

OR

10 a. What are the different steps used for simulation and synthesis?

(08 Marks)

b. Mention different styles of descriptions in HDL. Write a short note on behavioral description and also HDL code for half adder using behavioral description. (08 Marks)

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