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10CS46

**Fourth Semester B.E. Degree Examination, Dec.2017/Jan.2018**  
**Computer Organization**

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting at least TWO questions from each part.**

**PART - A**

- 1 a. With a neat block diagram, explain the different functional units of a digital computer. (06 Marks)  
b. Explain how byte addressability can be achieved using little endian and big endian memory representation. Write an example for each. (06 Marks)  
c. Perform the following operations on the 5-bit signed numbers using 2's complement representation system. Also indicate whether overflow has occurred or not.  
i)  $(-10) + (-13)$   
ii)  $(-10) - (+4)$   
iii)  $(-3) + (-8)$   
iv)  $(-10) - (+7)$ . (08 Marks)
- 2 a. Define Addressing Mode, explain the following addressing modes with an example and also show the effective address in each case?  
i) Absolute  
ii) Indirect  
iii) Index (10 Marks)  
b. Illustrate and explain with neat diagrams and examples, how logical shift and rotate instructions are implemented? (10 Marks)
- 3 a. What do you mean by interrupt? Explain polling and vectored interrupts. (06 Marks)  
b. Define bus arbitration. Explain the centralized arbitration with a neat diagram. (06 Marks)  
c. What is DMA? Explain how the DMA controllers are used in a computer system. (08 Marks)
- 4 a. Explain the following with respect to USB :  
i) Characteristics  
ii) Architecture  
iii) Addressing. (10 Marks)  
b. Discuss the main phases involved in the operation of SCSI bus. (08 Marks)  
c. Differentiate between serial port and parallel port. (02 Marks)

**PART - B**

- 5 a. With the help of a neat block diagram, explain the working of a  $1K \times 1$  memory cell organization. (10 Marks)  
b. Explain the memory hierarchy with respect to speed, size and cost with a neat diagram. (05 Marks)  
c. With a block diagram, explain the working principle of direct mapping cache memory. (05 Marks)

- 6 a. Discuss with a neat diagram, the design of a 4-bit carry-look ahead adder. (10 Marks)  
b. Perform multiplication for +13 and -6 using Booth's Algorithm. (05 Marks)  
c. With a neat figure, explain the circuit arrangement for binary division. (05 Marks)
- 7 a. List out the actions needed to execute the instruction Add (R<sub>3</sub>), R<sub>1</sub>. Write and explain sequence of control steps for execution of the same. (10 Marks)  
b. With a neat block diagram, explain hardwired control unit. Show the generation Z<sub>in</sub> and End control signals. (10 Marks)
- 8 a. With a neat diagram, explain the organization of a shared memory multi processor. (08 Marks)  
b. What is hardware multithreading? Explain the two approaches to hardware multithreading. (08 Marks)  
c. Discuss: i) SISD ii) SIMD iii) MIMD iv) MISD. (04 Marks)

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