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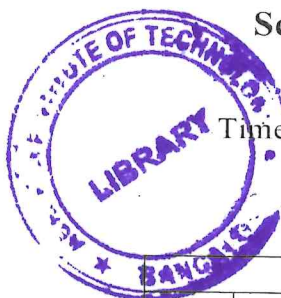
Seventh Semester B.E./B.Tech. Degree Examination, June/July 2026

Introduction to HDL

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.*



Module – 1				M	L	C
Q.1	a.	Explain the various types of parts available in VHDL and verilog with examples.	10	L2	CO1	
	b.	Write a sample programming verilog and VHDL and brief about the program constructs.	10	L1	CO1	
OR						
Q.2	a.	List and demonstrate the various types of arithmetic operators in VHDL and verilog.	10	L2	CO1	
	b.	Briefly explain Scalar and Composite type of data in VHDL with example each type.	10	L2	CO1	
Module – 2						
Q.3	a.	Show the constant declaration and assignment in VHDL with example and verilog.	10	L2	CO2	
	b.	Write and explain data flow program in verilog for full adder with truth table.	10	L3	CO2	
OR						
Q.4	a.	Write expression, truth table and circuit for 2 bit magnitude comparator with VHDL code.	10	L2	CO2	
	b.	Write expression, excitation table and circuit for D-Latch with VHDL code.	10	L2	CO3	
Module – 3						
Q.5	a.	Compare between signal assignment and variable assignment with an example.	10	L2	CO3	
	b.	Write syntax, flow chart and sample program for the following in VHDL i) if ii) if-else.	10	L2	CO3	

OR					
Q.6	a.	Write a program for 3-bit binary counter with synchronous clear in behaviour description using VHDL.	10	L2	CO3
	b.	Demonstrate Case X and Case Z statements with example in verilog.	10	L2	CO3
Module – 4					
Q.7	a.	Explain the following binding methods in VHDL with example i) Library and component ii) Library and module	10	L2	CO4
	b.	Write a VHDL program in structural description for 2×1 multiplexer.	10	L2	CO4
OR					
Q.8	a.	Write a code, logic diagram and truth table for 2×4 decoder in structural description.	10	L2	CO4
	b.	Write a verilog code in structural description for the 3-bit Ripple Carry Adder.	10	L2	CO4
Module – 5					
Q.9	a.	Describe the steps involved in designing Finite State Machine (FSM) with a suitable example.	10	L2	CO5
	b.	Design 3-bit synchronous counter using master slave JK F/F, sketch FSM and logic diagram and verilog code.	10	L2	CO5
OR					
Q.10	a.	Explain the following with example i) Generic ii) Parameter	10	L2	CO5
	b.	Write a structural description of an n-bit asynchronous down counter using general statement in verilog.	10	L2	CO5
