

CBCS SCHEME

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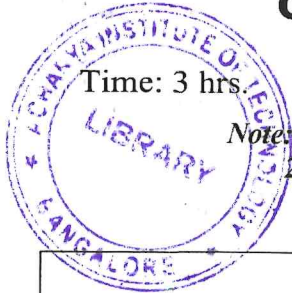
BMT304

Third Semester B.E./B.Tech. Degree Examination, June/July 2026 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

*Notes: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M: Marks, L: Bloom's level, C: Course outcomes.*



Module – 1			M	L	C
Q.1	a.	Draw and explain the connection between memory and processor with the respective registers.	10	L2	CO1
	b.	Describe the processes clock and performance equation with respect to performance of a computer.	10	L2	CO1
OR					
Q.2	a.	Draw and explain with block diagram basic functional units of a computer.	10	L2	CO1
	b.	Explain Big Endian and Little Endian with neat diagram.	10	L2	CO1
Module – 2					
Q.3	a.	Discuss with examples following addressing modes: i) Indirect Mode. ii) Indexing Mode. iii) Absolute Mode	10	L2	CO2
	b.	Explain logical shift operation with example.	10	L2	CO2
OR					
Q.4	a.	Discuss the following in case of subroutine: i) Subroutine Nesting ii) Parameter Passing.	10	L2	CO2
	b.	Explain PUSH and POP instruction with example.	10	L2	CO2
Module – 3					
Q.5	a.	Explain hardware interrupt with diagram.	10	L2	CO3
	b.	Explain with neat diagram the implementation of interrupt priority using individual interrupt request and acknowledge lines.	10	L2	CO3

OR					
Q.6	a.	Discuss how simultaneous interrupt request from several I/O devices will be handled by a processor through a single INTR line.	10	L2	CO3
	b.	Draw the diagram of DMA controller interface in a computer system and its working principle.	10	L2	CO4
Module – 4					
Q.7	a.	Explain SRAM cell and DRAM and explain the read/write operation.	10	L2	CO4
	b.	Sketch the organization of 16×8 memory chip.	10	L2	CO4
OR					
Q.8	a.	Classify various types of ROM.	10	L2	CO4
	b.	Explain secondary storage device, magnetic disk.	10	L2	CO4
Module – 5					
Q.9	a.	Explain single bus organization of data path with a neat diagram.	10	L2	CO5
	b.	Implement the control sequence needed for the execution of instruction ADD (R2), R1.	10	L2	CO5
OR					
Q.10	a.	Explain hardwired control unit organization in a processing unit.	10	L2	CO5
	b.	Demonstrate microprogrammed control unit organization in a processing unit.	10	L2	CO5
