

Third Semester B.E./B.Tech. Degree Examination, June / July 2026 Digital Logic Circuits

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks, L: Bloom's level, C: Course outcomes.*

Module – 1				M	L	C
Q.1	a.	Explain canonical minterm form and canonical maxterm form with an example.	06	L1	CO1	
	b.	Find the prime implicants and essential prime implicants of the following function. $f(a,b,c,d) = \sum m(0, 2, 5, 7, 8, 10, 13, 15) + \sum d(1, 4, 11, 14)$	06	L3	CO1	
	c.	Reduce the following function using K – map technique. i) $f(a, b, c, d) = \sum m(0, 1, 4, 8, 9, 10)$ ii) $f(a, b, c, d) = \pi M(0, 2, 3, 8, 9, 12, 13, 15)$	08	L2	CO1	
OR						
Q.2	a.	Find the reduced SOP form of the following function using NAND gates only. $F(a, b, c, d) = \sum m(4, 5, 6, 7, 8, 9, 10, 11)$	08	L2	CO1	
	b.	Simplify the following Boolean expression by using Quine Mc-cluskey minimization technique. $f(a,b,c,d) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$	12	L3	CO1	
Module – 2						
Q.3	a.	Implement the following using decoder 74138 : i) $F_1(a,b,c) = \sum m(2,6,7)$ ii) $F_2(a,b,c) = \pi m(1,2,4,6)$	06	L3	CO2	
	b.	Design full adder with truth table, K – map and logic diagram.	06	L3	CO2	
	c.	Explain with a neat diagram Look – ahead carry adder.	08	L2	CO2	
OR						
Q.4	a.	Design one – bit comparator with truth table and K – map.	10	L3	CO2	
	b.	Implement $u = \sum m(4, 5, 7, 9, 11, 12, 13, 15)$ using i) 8 – 1 MUX ii) 4 – 1 MUX	10	L3	CO2	
Module – 3						
Q.5	a.	Explain SR latch with circuit diagram, logic symbol and function table. Also explain application of SR latch.	10	L2	CO3	
	b.	With a neat circuit diagram explain working of a master slave JK flip – flop along with waveform.	10	L2	CO3	

OR

Q.6	a.	With a neat circuit diagram explain the working of master slave SR flip-flop along with waveform.	11	L2	CO3
	b.	Derive the characteristic equation for the following flip – flops : i) JK flip – flop ii) D – flip- flop iii) T flip – flop	09	L2	CO3

Module – 4

Q.7	a.	Explain universal shift register with neat circuit diagram.	10	L2	CO4
	b.	Design a synchronous mod – 6 counter using D flip – flop.	10	L3	CO4

OR

Q.8	a.	Explain binary ripple counter with neat circuit diagram, function table and waveform.	10	L2	CO4
	b.	Design a synchronous counter with a counting sequence 0, 1, 4, 6, 7, 5, 0 using JK flip – flop.	10	L3	CO4

Module – 5

Q.9	a.	Explain Mealy and Moore model with neat block diagram.	10	L2	CO5
	b.	Construct the transition table, state table and state diagram for the Mealy sequential circuit given below.	10	L3	CO5

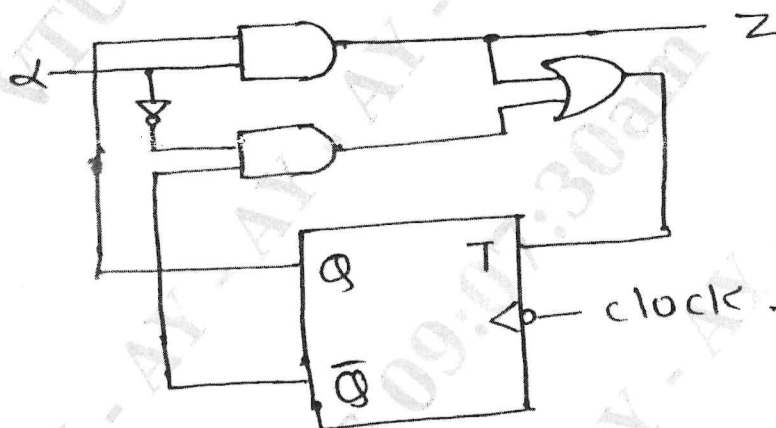


Fig. Q.9(b)

OR

Q.10	a.	Realize the system represented by the following state diagram using D flip – flop.	10	L3	CO5
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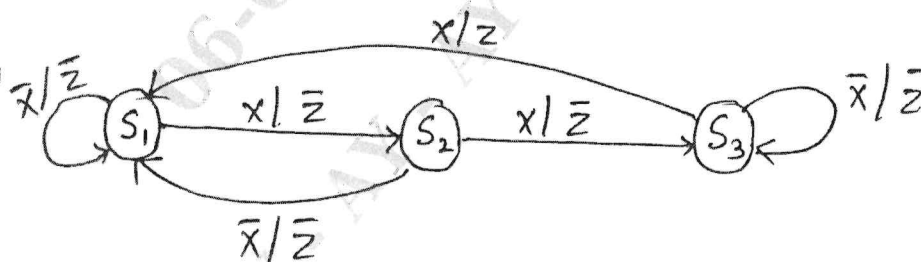


Fig. Q.10(a)

b.	Explain EPROM and flash memory.	10	L2	CO5
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