



CBCS SCHEME

21CS643

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2026 Advanced Computer Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Discuss the level of parallelism in the program execution on modern computer. (08 Marks)
- b. Illustrate a neat diagram the evaluation of computer architecture. (08 Marks)
- c. Discuss the hardware and software parallelism in a pipeline with neat diagram. (04 Marks)

OR

- 2 a. Solve the following fragment of a program of find the dependency: (08 Marks)

S ₁	Load	R ₁ ,	A	/ R ₁	← Memory (A) /
S ₂	Add	R ₂ ,	R ₁	/ R ₂	← (R ₁) + (R ₂) /
S ₃	Move	R ₁ ,	R ₃	/ R ₁	← (R ₃) /
S ₄	Store	B,	R ₁	/ Memory (B)	← (R ₁) /-

- b. Demonstrate any 2 Static Connections network briefly (08 Marks)
- c. Illustrate Vector Super Computer architecture briefly with a neat diagram. (04 Marks)

Module-2

- 3 a. Illustrate with a neat diagram the RISC architecture (10 Marks)
- b. Analyze the Pipelining Superscalar's processors, with a neat diagram. (10 Marks)

OR

- 4 a. Discuss the symbolic 3600 Lisp processor architecture. (10 Marks)
- b. Distinguish among Scalar and Vector Pipeline Execution. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-3

- 5 a. Discuss the features of backplane bus systems architecture with a neat diagram. (07 Marks)
- b. Compare and analyze central and distribution arbitration with relevant sketches. (07 Marks)
- c. For the given reservation table of three stage pipelining:

	1	2	3	4	5	6	7	8
S ₁	x					x		x
S ₂		x		x				
S ₃			x		x		x	

- i) What are the forbidden latencies and Collision vector?
- ii) Draw the State transition diagram.
- iii) List all simple cycles and greedy cycles.
- iv) Determine MAL.
- v) Determine the Pipeline throughput.

(06 Marks)

OR

- 6 a. Discuss the different mechanism for instruction pipelining, explain any one in details. (07 Marks)
- b. Analyze and explain direct Cache mapping Cache organization with its advantages and disadvantages. (07 Marks)
- c. Differentiate between CSA and CPA address Design a pipeline unit for fixed – point multiplication of 8-bit integers using CSA tree. (06 Marks)

Module-4

- 7 a. Discuss the cross bar network and cross point switch in multiprocessors system. (07 Marks)
- b. Illustrate the Hierarchical bus system with neat diagram. (07 Marks)
- c. Compare C-access memory organization Vs S-access memory organization (06 Marks)

OR

- 8 a. Illustrate with a neat diagram the concept of fine-grain multicomputer of MIT-J Machine, with MDP architecture. (07 Marks)
- b. Analyze snoopy protocols with its approaches. (07 Marks)
- c. Analyze and explain Hierarchical memory technique with neat diagram. (06 Marks)

Module-5

- 9 a. Define Parallel Programming Model. Illustrate any two parallel programming models. (07 Marks)
- b. Analyze the code given below and explain how to overcome from hazards using operand and forwarding techniques.
- Add $R_3 \leftarrow R_1 + R_2$
 Sub $R_5 \leftarrow R_4 - R_3$ (07 Marks)
- c. Demonstrate the different phases of parallelizing compiles with neat diagram. (06 Marks)

OR

- 10 a. Write a dependency testing and iteration space algorithm. Explain briefly. (07 Marks)
- b. Analyze the code given below and explain how to overcome from hazards using Register renaming technique: (07 Marks)
- DIV F_0, F_2, F_4
 ADD F_6, F_0, F_8
 SD $F_6, 0 (R_1)$
 SUB F_8, F_{10}, F_{14}
 MUL F_6, F_{10}, F_8
- c. Demonstrate Tomasulo's algorithm with a neat diagram briefly. (06 Marks)
