



CBCS SCHEME

BCS402

Fourth Semester B.E/B.Tech. Degree Examination, June/July 2026 Microcontrollers

Time: 3 hrs.

Max. Marks:100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Differentiate between CISC and RISC, and explain the four major rules of RISC design.	7	L2	CO1
	b.	Explain ARM core dataflow model and mention the different registers of ARM processor.	7	L2	CO1
	c.	Write a note on Exceptions, interrupts and the vector table.	6	L2	CO1
OR					
2	a.	With the help of basic layout diagram, explain the current program status register.	7	L2	CO1
	b.	With a neat diagram, explain embedded system software.	8	L2	CO1
	c.	What is pipeline in ARM? Explain the different pipeline stages of ARM 9 processor.	5	L2	CO1
Module – 2					
3	a.	Explain the different Data Processing Instruction in ARM.	10	L2	CO2
	b.	Briefly explain the different Load-Store Instruction categories used with ARM.	10	L2	CO2
OR					
4	a.	Discuss with proper syntax, the following : i) SWAP instruction ii) Software interrupt instruction.	10	L2	CO2
	b.	Write a C program that prints and square of the integers between 0 to 9 using function and explain how to convert this C function to an assembly function with command.	10	L2	CO2

Module – 3

5	a.	Discuss how registers are allocated to optimize the program in ARM processor.	10	L2	CO3
	b.	Write a note on portability issues in ARM.	10	L2	CO3

OR

6	a.	Explain the Load-Store instruction classes available by ARM architecture along with mapping C Datatypes.	10	L2	CO3
	b.	What is Pointer Aliasing? Explain function calls in ARM register.	10	L2	CO3

Module – 4

7	a.	What are interrupts or exceptions? Mentioning them, explain how they are handled in ARM processors.	7	L2	CO4
	b.	Explain the ARM firmware suite.	6	L2	CO4
	c.	Explain in detail the steps of a sandstone code structure.	7	L2	CO4

OR

8	a.	Explain Suitably, how FIQ and IRQ exceptions are enables and disabled in ARM processor.	10	L2	CO4
	b.	Explain Exception Priorities in detail with priority levels.	10	L2	CO4

Module – 5

9	a.	Explain with a neat diagram, memory hierarchy and cache memory.	8	L2	CO5
	b.	Write a note on Cache Line Replacement Policies.	6	L2	CO5
	c.	Discuss the relationship of a cache between processor core and main memory.	6	L2	CO5

OR

10	a.	Explain with a neat diagram, a four-way set associative cache to increase the set associatively.	9	L2	CO5
	b.	Write a note on allocation Policy on a Cache Miss.	6	L2	CO5
	c.	Brief out measuring of Cache Efficiency.	5	L2	CO5
