



Third Semester B.E./B.Tech. Degree Examination, June/July 2026 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, explain the basic operational concepts of computer. (06 Marks)
- b. Write a program to evaluate arithmetic expression $X = (A + B) * (C + D)$. (08 Marks)
 - i) Using three address instruction
 - ii) Using two address instruction
 - iii) Using one address instruction
 - iv) Using zero address instruction.
- c. Describe the below addressing modes with examples. (06 Marks)
 - i) Immediate Mode
 - ii) Auto increment and Auto Decrement Mode
 - iii) Direct and Indirect Address Mode.

OR

- 2 a. Give the comparison between memory mapped I/O and I/O mapped I/O. (06 Marks)
- b. Explain Big-Endian and Little-Endian methods of byte addressing with example. (06 Marks)
- c. Register R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instruction (08 Marks)
 - i) Add - (R₂), R₅
 - ii) Sub (R₁) +, R₅
 - iii) Load 20(R₁), R₅
 - iv) Store R₅, 30(R₁, R₂).

Module-2

- 3 a. What is Bus Arbitration? Explain the distributed bus Arbitration with a neat diagram. (08 Marks)
- b. Draw a neat timing diagram and explain Multicycle synchronous bus transfer for read operation. (06 Marks)
- c. What are Exception? Point out and explain the different kinds of exceptions. (06 Marks)

OR

- 4 a. Discuss the following methods of handling interrupts from multiple devices.
 i) Interrupt nesting/priority structure
 ii) Daisy chain method. (08 Marks)
- b. Demonstrate the DMA and its implementation and show how the data is transferred between memory and I/O device using DMA controller. (07 Marks)
- c. Explain the general 8 bit parallel interface circuit with a neat diagram. (05 Marks)

Module-3

- 5 a. Explain the internal organization of a $2m \times 8$ dynamic memory chip with a neat diagram. (08 Marks)
- b. What is virtual memory? Explain how virtual memory is translated with a neat diagram. (08 Marks)
- c. Define the following :
 i) Memory latency
 ii) Memory bandwidth. (04 Marks)

OR

- 6 a. Explain the direct mapped cache in the mapping function with a neat diagram. (08 Marks)
- b. Describe the organization of an $2m \times 32$ memory using $512K \times 8$ memory chip. (08 Marks)
- c. What is ROM? Point out and explain various types to ROM. (04 Marks)

Module-4

- 7 a. Convert the following pairs of decimal numbers to 5 bit, signed, 2's complement, binary numbers and add them. State whether or not overflow occurs in each case
 i) 5 and 10 ii) -14 and +11 iii) -5 and 7 iv) -10 and -13. (08 Marks)
- b. Draw a neat diagram of carry look ahead adder and explain. (08 Marks)
- c. With a neat diagram show how the addition and subtraction of n bit no is performed. (04 Marks)

OR

- 8 a. Explain the concept of carry –save addition for the multiplication operation $M \times Q = P$ for 4-bit operand with diagram and suitable example. (08 Marks)
- b. Multiply each of the following pairs of signed 2's complement number using Booth algorithm. A = multiplicand B = multiplier.
- i) A = 010111 B = 110110
 - ii) A = 11 0011 B = 101100
 - iii) A = 110101 B = 011011
 - iv) A = 001111 B = 001111
- (08 Marks)
- c. Give the control sequence for the execution of instruction Add(R₃), R₁? (04 Marks)

Module-5

- 9 a. What is pipeline? Explain 4 stage pipeline with its instruction execution steps and hardware organization? (10 Marks)
- b. Write about the following concepts
- i) Vector processing
 - ii) Array processors.
- (10 Marks)

OR

- 10 a. What is Instruction Pipelining? What are the conflicts that occurred during instruction pipelining? (10 Marks)
- b. Explain popular Flynn categories. (10 Marks)
