



CBCS SCHEME

21CS33

Third Semester B.E./B.Tech. Degree Examination, June/July 2026 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Derive the expressions for fixed bias circuit, with neat diagram. Also show the load line analysis. (10 Marks)
- b. Explain the Parameters of Regulated Power Supply. (10 Marks)

OR

- 2 a. With neat diagram explain successive approximation ADC method. (10 Marks)
- b. With the help of neat diagram, explain principle of Relaxation Oscillator. (10 Marks)

Module-2

- 3 a. Find all the prime implicants and essential prime implicants by reducing following function using K-map.
 $F(abcd) = \sum m(0, 1, 6, 7, 8, 9, 12, 13, 14, 15)$ (10 Marks)
- b. Reduce the following function using K-map and implement the expression using basic gates.
 $F(abcd) = \sum m(0, 2, 5, 7, 8, 10, 13, 15) + \sum d(1, 4, 11, 14)$ (10 Marks)

OR

- 4 a. Find the minimal sum of following function using QM method.
 $f(abcd) = \sum m(3, 4, 5, 7, 10, 12, 14, 15) + \sum d(2)$ (10 Marks)
- b. Simplify the following function using Petrick's method.
 $f(abcd) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$ (10 Marks)

Module-3

- 5 a. Define Hazards. With example explain different types of hazards. (10 Marks)
- b. Implement the following Boolean function using 8:1 MUX.
 $F(ABCD) = \sum m(0, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 15)$ (10 Marks)

OR

- 6 a. Design full adder and full subtractor circuit using 8:1 MUX. (10 Marks)
- b. Design Binary to Gray code converter using Decoder. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Explain the structure of VHDL and write the verilog code for following circuit using structural model [Refer Fig.Q7(a)].

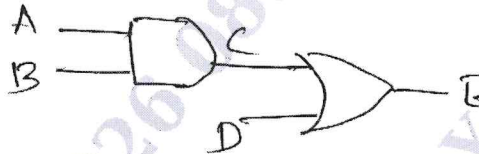


Fig.Q7(a)

(10 Marks)

- b. Explain conditional signal assignment statement. Write verilog code for 8:1 MUX. (10 Marks)

OR

- 8 a. Explain JK master slave flip flop with neat diagram. (10 Marks)
- b. Give characteristic equations for SR, JK, and T Flip-flop with excitation table. (10 Marks)

Module-5

- 9 a. Explain parallel adder with accumulator. (10 Marks)
- b. Explain SISO shift register. (10 Marks)

OR

- 10 a. Design mod-6 synchronous counter using JK flip-flop. (10 Marks)
- b. Design synchronous counter to count the sequence
0 – 4 – 7 – 2 – 3 – 0 using SR flip-flop. (10 Marks)
