CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026

Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define the following : i) Canonical SOP ii) Canonical POS iii) Essential Prime Implicant (EPI) iv) Prime Implicant (PI) v) Min term and Max term with a table of two input variable representation	10	L1	CO1
	b.	Using Quine Mccluskey method and PI reduction table, determine the minimal SOP expression for the following function. $Y = f(a, b, c, d) = \Sigma(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$	10	L3	CO1
		OR			
Q.2	a.	Explain the procedure to place SOP and POS equations into canonical form convert the following equations into canonical forms i) $T = f(a, b, c) = (a + b')(b' + c)$ ii) $G = f(w, x, y, z) = w'x + yz'$	10	L3	CO1
	b.	Solve the given functions using Kamangh Map i) $F = f(w, x, y, z) = \Sigma(0, 7, 8, 9, 10, 12) + \Sigma d(2, 5, 13)$ ii) $G = f(a, b, c, d) = \pi(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ Also identify the prime implicants.	10	L3	CO1
		Module – 2			
Q.3	a.	Implement the function using multiplexers i) $f(x, y, z) = \Sigma m(0, 2, 3, 5)$ using 4×1 multiplexer ii) $f(w, x, y, z) = \Sigma m(0, 1, 5, 6, 7, 9, 12, 15)$ using 8×1 multiplexer.	10	L2	CO2
	b.	Explain the concept of carry look ahead adder with related equation and block diagram.	10	L2	CO2
		OR			
Q.4	a.	Using a 4-bit binary adder, design a logic to convert a decimal digit in 8421 code into a decimal adder.	10	L3	CO2
	b.	Implement the following functions using 3 : 8 decoder. i) $P = f(w, x, y, z) = \Sigma(1, 4, 8, 13)$ $Q = g(w, x, y, z) = \Sigma(2, 7, 13, 14)$ ii) $A = f(x, y, z) = \pi(0, 1, 3, 5)$ $B = f(x, y, z) = \Sigma(1, 4, 5, 7)$	10	L3	CO2

<table>
<tr><td colspan="6">Module – 3</td></tr>
<tr><td>Q.5</td><td>a.</td><td>Explain master slave JK flip-flop with the help of circuit diagram and timing diagrams.</td><td>10</td><td>L2</td><td>CO3</td></tr>
<tr><td></td><td>b.</td><td>Design a synchronous Mod -6 counter with sequence 0-2-3-6-5-1 using JK flip-flop.</td><td>10</td><td>L3</td><td>CO3</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>Q.6</td><td>a.</td><td>Design a 4-bit binary ripple up counter with logic diagram and counting sequence and explain its operation.</td><td>10</td><td>L3</td><td>CO3</td></tr>
<tr><td></td><td>b.</td><td>With the help of logic diagram and counting sequence, explain.
i) Ring counter
ii) Mod – 8 twisted ring counter.</td><td>10</td><td>L2</td><td>CO3</td></tr>
<tr><td colspan="6">Module – 4</td></tr>
<tr><td>Q.7</td><td>a.</td><td>What are the different data types in verilog. Explain with examples.</td><td>10</td><td>L2</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>i) Develop a verilog program to implement 2×1 multiplexer using conditional operator. Also write the truth table of 2×1 mux
ii) Design a 2×1 multiplexer using dataflow verilog description draw a logic diagram and logic gate level circuit for it.</td><td>4

6</td><td>L3

L3</td><td>CO4

CO4</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>Q.8</td><td>a.</td><td>Discuss in detail different description styles in verilog.</td><td>8</td><td>L2</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>Let A = 5' b11011, B = 5' b 10101 C = 4' d3
Determine the output the following verilog statements.
i) d = & A ii) e = ~^ 4' b1011 iii) f = ~ (A & (~B))
iv) g= A| |B v) b = 3** 2 vi) i = {2{A}}</td><td>12</td><td>L3</td><td>CO4</td></tr>
<tr><td colspan="6">Module – 5</td></tr>
<tr><td>Q.9</td><td>a.</td><td>Design a 4-bit counter with synchronous hold using verilog. Also draw the simulation waveform.</td><td>10</td><td>L3</td><td>CO5</td></tr>
<tr><td></td><td>b.</td><td>Explain the operation of positive edge triggered JK flip-flop by using a verilog code using case statement. Write truth table and timing diagram.</td><td>10</td><td>L2</td><td>CO5</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>Q.10</td><td>a.</td><td>Explain the operation of half adder and implement using structural description in verilog.</td><td>6</td><td>L2</td><td>CO5</td></tr>
<tr><td></td><td>b.</td><td>Write the verilog format of case statement and explain.</td><td>4</td><td>L2</td><td>CO5</td></tr>
<tr><td></td><td>c.</td><td>Develop a verilog behavioral description for 3 bit binary up counter.</td><td>6</td><td>L3</td><td>CO5</td></tr>
<tr><td></td><td>d.</td><td>Develop a verilog program for D latch using behavioral description style.</td><td>4</td><td>L3</td><td>CO5</td></tr>
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