

# CBCS SCHEME

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BETCK205J

**Second Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026**  
**Introduction to Embedded System**

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
 2. M : Marks , L: Bloom's level , C: Course outcomes.*

Module – 1			M	L	C
Q.1	a.	Classify Embedded Systems based on i) Complexity and Performance requirement      ii) Generation	6	L2	CO1
	b.	With a neat diagram, explain elements of Embedded Systems.	8	L2	CO1
	c.	Write a short note on following external communication interfaces : i) USB      ii) Bluetooth      iii) Wi-Fi.	6	L1	CO1
<b>OR</b>					
Q.2	a.	Differentiate between General purpose computing system and Embedded system.	6	L2	CO1
	b.	Identify different core categories used as core in embedded systems.	8	L2	CO1
	c.	Write a short note on following on-board communication interface buses: i) I2C      ii) SPI.	6	L1	CO1
<b>Module – 2</b>					
Q.3	a.	Explain operational quality attributes of an Embedded System.	10	L2	CO3
	b.	Develop a functional model of washing machine by considering it as an application specific embedded system.	10	L3	CO3
<b>OR</b>					
Q.4	a.	Explain Non-operational quality attributes of an Embedded System.	10	L2	CO3
	b.	Develop a functional model of car by considering it as an application of automotive embedded system.	10	L3	CO3
<b>Module – 3</b>					
Q.5	a.	Analyze fundamental issues in Hardware Software Co-design.	8	L2	CO3
	b.	Design an FSM for automatic seat belt warning system.	8	L3	CO5
	c.	With a neat IC pin diagram and truth table, explain the multiplexer (74LS151).	4	L1	CO3
<b>OR</b>					
Q.6	a.	Design an embedded system for Automatic Coffee/Tea vending machine.	8	L3	CO5
	b.	With a neat diagram, explain the HDL-based VLSI design flow.	8	L2	CO3
	c.	Compare Combinational and Sequential circuits.	4	L2	CO3

## Module – 4

Q.7	a.	Explain the super loop-based approach for embedded firmware design. Write a pseudo-code.	6	L2	CO4
	b.	With a neat diagram, explain the conversion of Assembly language to Machine language conversion process. List the advantages and drawbacks of assembly language based development.	8	L2	CO4
	c.	List and explain different types of files generated on cross-compilation.	6	L2	CO4

## OR

Q.8	a.	With a neat diagram, explain the conversion of high-level language to machine language conversion process. List the advantages and drawbacks of high-level language based development.	8	L2	CO4
	b.	What do you mean by simulator? List the features of simulators. Mention the advantages and drawbacks of simulator-based debugging.	6	L1	CO2
	c.	Explain In Circuit Emulator (ICE) with neat diagram.	6	L2	CO2

## Module – 5

Q.9	a.	With a neat diagram of OS architecture explain Kernel services.	6	L2	CO2
	b.	With a neat diagram, explain Monolithic and Microkernel. Mention the advantages and drawback of each.	6	L2	CO2
	c.	In a Preemptive Priority based scheduler three processes with process IDs P1, P2, P3 with estimated completion times 10, 5, 7 milliseconds and priorities 1, 3, 2 (0-highest priority, 3-lowest priority) respectively enter the ready queue together. A new process P4 with estimated completion time 6 ms and priority 0 enters the 'Ready' queue after 5 ms of the start of execution of P1. Assume all the processes contain only CPU operations and no I/O operations are involved. Calculate Average Waiting and Average Turn Around Time.	8	L3	CO5

## OR

Q.10	a.	Differentiate General purpose OS and RTOS. Give example for each.	6	L2	CO2
	b.	Explain the process and states of process using a state transition diagram.	6	L2	CO2
	c.	In a Preemptive Shortest Job First (SJF) scheduler, three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds, respectively, enter the ready queue together. A new process P4 with an estimated completion time 2 ms enters the ready queue after 2 ms. Assume all the processes contain only CPU operation and no I/O operations are involved. Calculate Average Waiting Time and Average Turn – Around Time.	8	L3	CO2

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